MODELING, DESIGN, AND DEMONSTRATION OF 2.5-D GLASS INTERPOSER PACKAGES FOR HIGH PERFORMANCE COMPUTING APPLICATIONS

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MODELING, DESIGN, AND DEMONSTRATION OF 2.5-D GLASS INTERPOSER PACKAGES FOR HIGH PERFORMANCE COMPUTING APPLICATIONS

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For the gospel's sake… I Corinthians 9:23

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LIST OF SYMBOLS AND ABBREVIATIONS

α	Transmission line attenuation
A	Conductor cross section
AFR	Auto fixture removal
AR	Copper height to line width ratio
BEOL	Back-end of line
BER	Bit error rate
BGA	Ball grid array
c	Capacitance per unit length
C2P	Chip-to-package bump pitch
CLI	Chip-level interconnect
CMP	Chemical mechanical planarization
CPW	Co-planar waveguide
CPU	Central processing unit
CTE	Coefficient of thermal expansion
δ	Interconnect density
DDR	Double data rate
DFE	Digital feedback equalization
DFR	Dry film photoresist
DFT	Designs for test
DRAM	Dynamic random-access memory
ε_r	Dielectric relative permittivity
e-less	Electroless
EMIB	Embedded multi-die interconnect bridge
EIC	Embedded interposer carrier
ENIG	Electroless nickel immersion gold
FC-BGA	Flip chip ball grid array

FPGA	Field programmable gate array
GHz	Gigahertz
GPU	Graphics processing unit
HBM	High bandwidth memory
HF	Hydrofluoric acid
HPC	High performance computing
HVM	High volume manufacturing
I/O	Input/Output
IC	Integrated circuit
ILD	Inter-layer dielectric
ISI	Inter-symbol interference
λ	Wavelength
l	Inductance per unit length
L_1	Critical interconnect length for inductive signal behavior
L_2	Critical interconnect length for Capacitive signal behavior
LTCC	Low temperature co-fired ceramic
MSL	Microstrip transmission line
NRZ	Non-return to zero
NSMD	Non-solder mask defined
PDN	Power delivery network
PID	Photo-imageable dielectric
PNA	Performance network analyzer
pS	Differential pair spacing
PVD	Physical vapor deposition (sputter)
PWB	Printed wiring board
r	Resistance per unit length
Ra	Average surface roughness
RDL	Redistribution layer
σ	Bulk conductivity

S-Parameter	Scattering parameter
SAP	Semi-additive process
SBU	Sequential build-up
S_{DD11}	Differential return loss
S_{DD21}	Differential insertion loss
SL	Stripline transmission line
SMD	Solder mask defined
SoC	System on Chip
SOLT	Short-open-load-thru
SRO	Solder resist opening
SSI	Stacked silicon integration
SSN	Simultaneous switching noise
tanδ	Dielectric loss tangent
TCB	Thermo-compression bond
td	Interconnect delay per unit length
TD	Interconnect delay measured at 50% V_{IN}
Ti-Cu	Titanium-copper
TPV	Through package via
TSV	Through silicon via
UBM	Under bump metallurgy
UI	Bit unit interval
VNA	Vector network analyzer
Z0	Characteristic Impedance
Z_{diff}	Differential characteristic impedance

SUMMARY

The objective of this research was to model, design, fabricate, and characterize high density, die-to-die and high speed, die-to-board interconnections in 2.5-D glass interposer packages for high performance computing. Transistor scaling is reaching fundamental and economic limits below the 14 nm node, and bandwidth between logic and memory is approaching a memory wall due to power and latency overheads associated with high speed channels on board. Heterogeneous multi-die integration by 3-D IC stacking with fine pitch through silicon vias has been extensively researched to address these scaling and performance challenges, but thermal dissipation limited 3-D IC to lower power mobile applications. For high performance computing applications, 2.5-D interposers with high density interconnections between two or more die, which are assembled side-by-side on the same substrate, have emerged as the preferred approach to address transistor scaling challenges and to improve bandwidth without significantly increasing signal power and latency compared to 3-D IC.

The first commercial application of a 2.5-D interposer was a split-die, partitioned field-programmable gate array integrated on a back-end of line (BEOL) silicon interposer by Xilinx. This packaging architecture was further engineered by AMD to integrate a graphics processing unit with high bandwidth memory. Silicon interposers had two major challenges—high electrical loss and high packaging cost. Organic interposers are being developed to address these and other silicon interposer challenges. Poor dimensional stability and warpage of organic laminates, however, limited interconnect scaling compared to BEOL dimensions.

Glass packaging presents a unique opportunity to optimally scale bandwidth, power, and cost to become the next generation electronic packaging material following ceramics (1970's – '80's) and organics (1990's – 2000's). Low dielectric constant and low loss tangent of glass reduces electrical loss. Smooth surface finish, low total thickness variation, high elastic modulus, and exceptional dimensional stability of glass enables scaling of redistribution layer (RDL) line width to 2 μm and beyond on large panels. Tailored coefficient of thermal expansion, which is dependent on glass composition, facilitates direct attachment of the glass package to the system board while maintaining chip- and board-level interconnect reliabilities without an organic ball grid array substrate.

The 2.5-D glass interposer package designed in this thesis offers the best combination of low-loss, fine-pitch interconnects and panel-scalable, double-sided fabrication processes to improve signal integrity and to reduce packaging cost compared to wafer-based silicon interposers. Specifically, this thesis addressed two major glass interposer electrical design challenges: (1) high density, die-to-die (wide I/O) interconnects with lower latency than BEOL silicon interconnects, and (2) high speed, die-to-board (external I/O) interconnects with lower attenuation than through silicon via.

Modeling, design, fabrication, and characterization of 2.5-D glass interposer RDL demonstrated a 2x reduction in wide I/O latency and a 10x reduction in external I/O attenuation compared to BEOL RDL. This electrical design research was used as a design guideline in the first 2.5-D glass interposer demonstration that integrated RDL and chip assembly processes developed by other researchers to achieve 6 μm pitch RDL and 56

μm chip-level interconnect pitch fabricated on a 100 μm thick 150 mm x 150 mm glass panel with through package via.

CHAPTER 1. INTRODUCTION

Future bandwidth requirements for high performance computing (HPC) systems running the cloud and edge infrastructures are being driven by emerging technologies including: Internet-of-Things, smart infrastructures, and autonomous electric vehicles. A 60% increase in the number of connected devices is expected from 2015 through 2020 and requires an exponential increase in data center traffic over this same time frame as depicted in Figure 1 [1-3]. As a result, core network switch and router bandwidth is

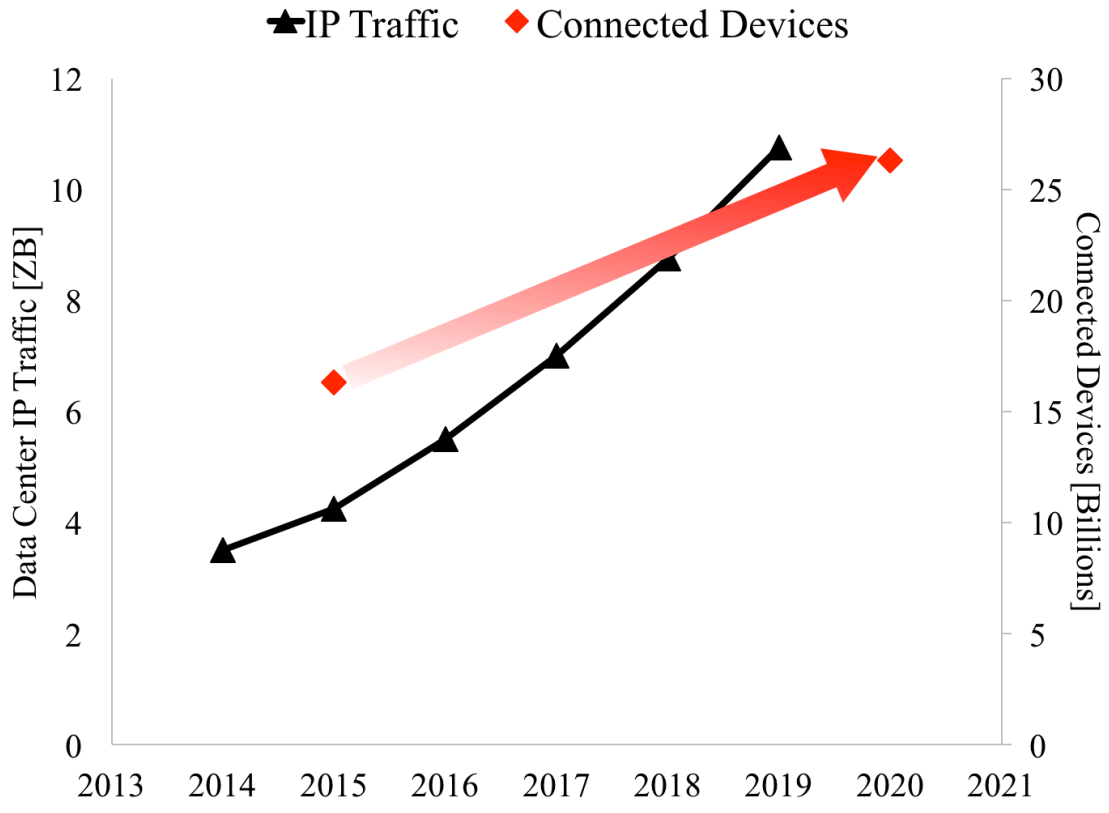


Figure 1. Trend in network traffic as a result of connected devices [1].

expected to increase by 2 – 10x per technology generation [4].

At the same time, performance and cost benefits of transistor scaling according to Moore's law slowed at the 14 nm IC node. Specifically, transistor scaling increased die defect density before maturing to high volume manufacturing (HVM) leading to low yield at large die size. Increased performance by way of transistor scaling and interconnection by standard input/output (I/O) between flip chip ball grid array (FC-BGA) packages on board was no longer sufficient to meet HPC requirements [2, 5]. Challenges for standard I/O to meet performance demands included density, signal power, and scalability [3]. Large dies were partitioned and integrated on package to address these cost and performance challenges [6]. Therefore, microsystems packaging became as important as on-chip scaling for highest performance at lowest power and cost [7]. Advanced packaging was needed to meet system requirements by closing the system scaling gap. The system scaling gap referred to the large disparity between semiconductor package ($1x10^3$ I/O per cm^2) and chip ($1x10^8$ I/O per cm^2) interconnection density [7, 8]. Hence, increasing package interconnect density to improve system throughput was critical to enable next generation electronics.

Advanced packaging architectures such as 3-D IC stacking and 2.5-D interposers have been adopted to increase bandwidth and to reduce signal power by 10-1000x. Due to the thermal and cost challenges associated with 3-D IC stacking, 2.5-D interposers with side-by-side heterogeneous die integration became the primary architecture for HPC systems that require greater than 50 – 100 W per chip [9]. The main advantages of integration on package using 2.5-D interposer was system miniaturization, performance, power, and heterogeneous integration [10]. Side-by-side IC integration on a 2.5-D

interposer necessitated aggressive chip-level interconnect (CLI) and redistribution layer (RDL) pitch scaling to increase interconnection density comparable to on-chip back-end of line (BEOL) interconnections. Various 2.5-D silicon and organic interposer technologies were developed to increase interconnection density and are reviewed in 0. This thesis research demonstrates two electrical design fundamental building blocks—low latency die-to-die and low loss die-to-board interconnections—integrated for the first time on a 2.5-D glass interposer package to address the performance and cost challenges of silicon interposers, as well as interconnect density challenges of organic package substrates and interposers.

1.1 Packaging Requirements for High Performance Computing

System throughput—ultimately determined by bandwidth between logic and memory—is the key figure of merit for any high performance computing system. High performance system packages that integrate logic and memory must consider the following parameters to increase system throughput:

1. Interconnection density.
2. Interconnection length.
3. Power consumption.
4. System reliability.
5. System cost.

Die-to-die bandwidth BW is proportional to the number of channels and data rate per channel according to Equation 1 and shown in Figure 2 where δ is the number of interconnects per unit length per packaging layer, w is the signal bus width, N is the

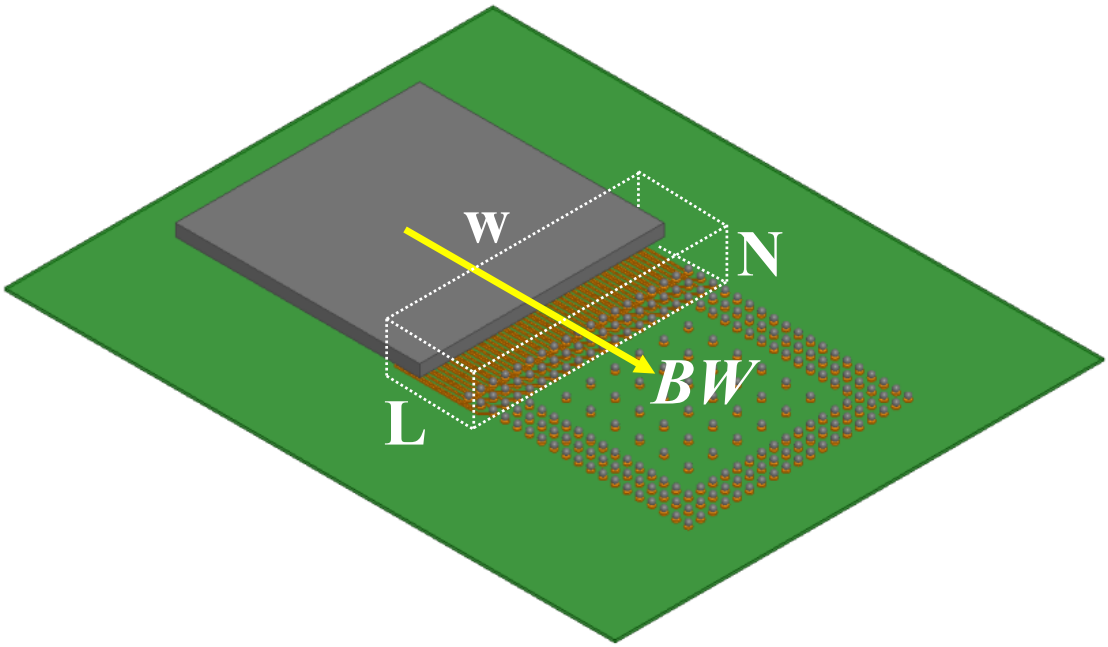


Figure 2. Die-to-die bandwidth schematic.

number of signal layers, and r is the data rate per channel (with an inherent dependence on L—the interconnect length between die).

$$BW = \delta wN \cdot r \tag{1}$$

Improving bandwidth between ICs requires either high speed serial links, or low speed parallel channels based on Equation 1. In the former, the number of interconnections is low, while the data rate is increased. This approach is best exemplified by the progression of double data rate (DDR) dynamic random-access memory (DRAM) bandwidth summarized in Figure 3.

Logic and memory integration on board using DDRx-DRAM is fast approaching a memory wall due to increased signal power and latency [11]. Alternatively, bandwidth can be improved by increasing interconnection density, while maintaining a relatively low data rate per channel. This approach is realized by the introduction of high bandwidth memory (HBM) where logic and memory are integrated on a package using a wide I/O interface to dramatically improve bandwidth relative to DDR DRAM [12].

Integrating multiple ICs on a single package shortens channel length and reduces signal power and latency compared to standard I/Os between individually packaged ICs

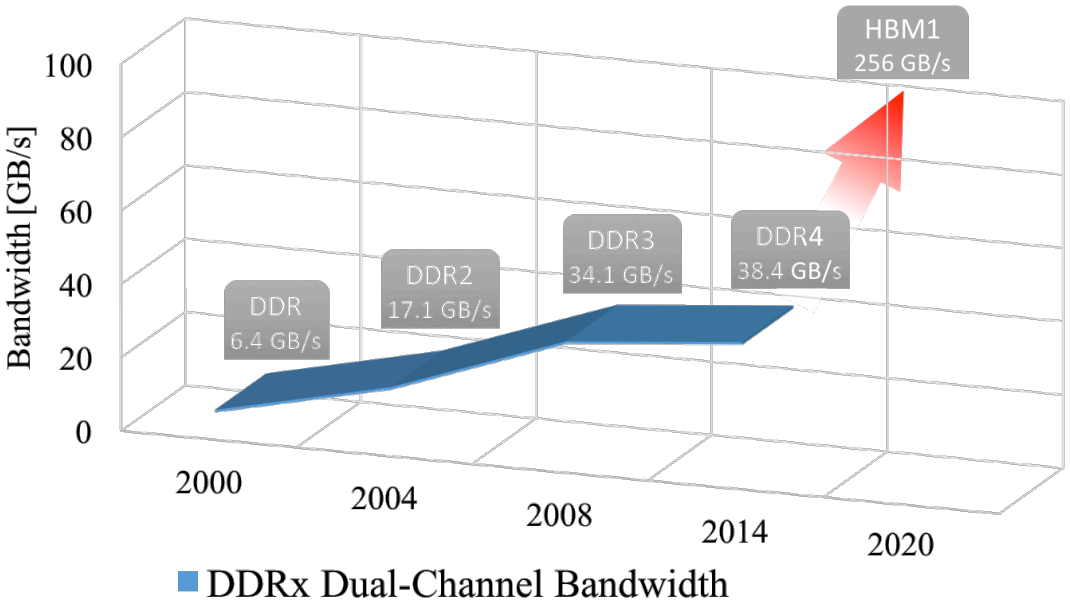


Figure 3. DDRx-DRAM aggregate bandwidth compared to high bandwidth memory.

on board [5]. Therefore, increased bandwidth by integrating ICs on package with high density interconnections has been the key focus to increase throughput in high performance computing.

Chip-level bump pitch below 50 μm combined with RDL line pitch below 10 μm is required for wide I/O [13]. Leading edge FC-BGA packages use organic substrates that are limited to 100 – 120 μm bump pitch. An interposer, typically silicon, is added between the die and package substrate to scale bump pitch and increase interconnection density between ICs. The introduction of an additional packaging layer, however, reduces signal and power integrity. Signal integrity is degraded by the added signal length and impedance discontinuities for external I/O. External I/Os are required to connect with external system components, and are typically 28 – 56 Gbps interfaces with stringent loss and timing budgets. Power integrity is affected by an increase in parasitic resistance and inductance in the power delivery network (PDN) leading to increased simultaneous switching noise (SSN) due to high plane impedance at resonant frequencies [14]. Furthermore, the interposer increases the risk of thermo-mechanical reliability failures and cost at the system level.

Considering the aforementioned parameters, the important packaging characteristics for high performance computing to increase system throughput are:

- High interconnection density between two or more ICs.
- Short signal length between ICs integrated on a single package.
- Reduced packaging layers between the die and printed wiring board (PWB).

An electronic package that maximizes system reliability and minimizes system costs while addressing these characteristics is critical to meeting future system needs at lowest costs.

1.2 3-D IC Stacking and 2.5-D Interposers for High Bandwidth

Heterogeneous multi-die integration on a single package to improve bandwidth was best accomplished in one of two ways: (1) 3-D IC vertical stacking or (2) 2.5-D side-by-side assembly as shown Figure 4 and Figure 5 respectively.

Although 3-D IC stacking with through silicon vias (TSV) enabled the shortest interconnection length on the order of 50 µm – 100 µm, it had significant challenges such

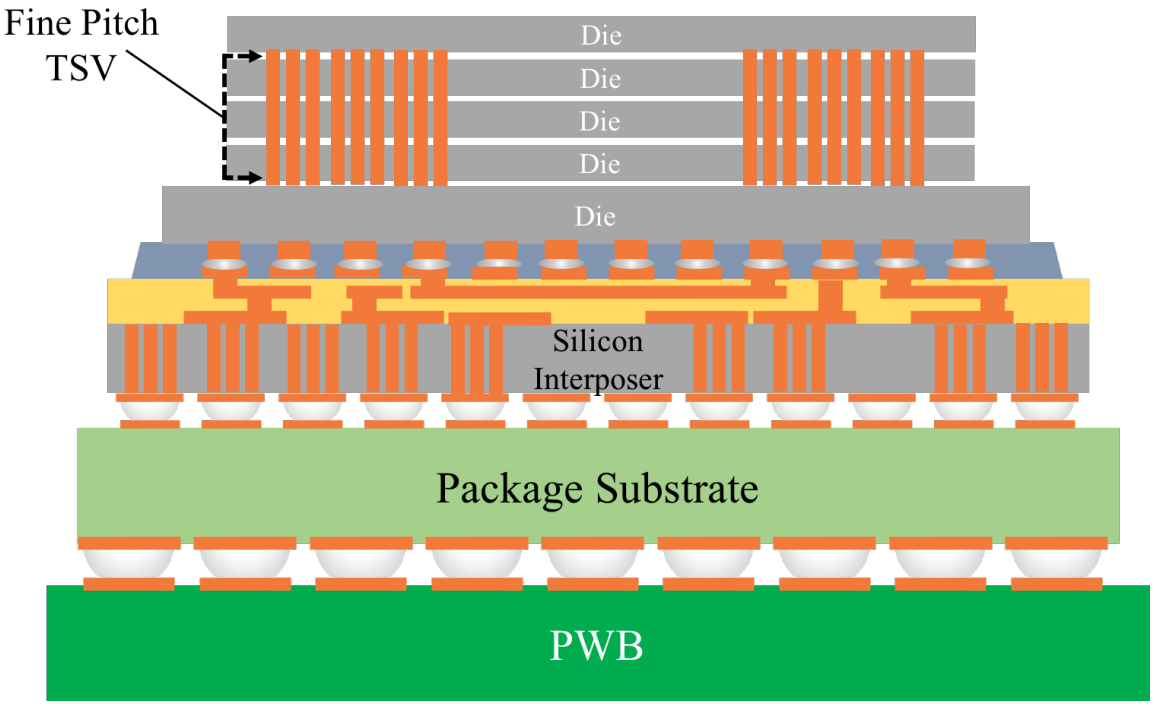


Figure 4. 3D-IC package with fine pitch TSV.

as thermal keep out zones, TSV cost and reliability, and power delivery. Furthermore, TSV-based direct chip stacking faced power scaling limits due to thermal crosstalk between ICs affecting device temperature and performance. These fundamental challenges have made 2.5-D interposers the primary choice for high performance IC integration on package [9]. A 2.5-D interposer refers to the integration of two or more ICs assembled in close proximity on a high density substrate and interconnected by RDL at line pitch and width comparable to on-chip wiring—significantly smaller than the 10 μm line and space of state of the art FC-BGA substrates [15].

Given this packaging architecture, the electrical design of a 2.5-D interposer must consider the following signal regimes:

1. High density, wide I/O channels on the interposer between ICs.
2. High speed, external I/O channels from the ICs to board.

Wide I/O channel density determines 2.5-D interposer RDL line pitch and width and chip-level interconnection pitch. External I/O data rate determines loss, crosstalk, and timing budgets. In general, the performance of wide I/O is improved with decreased line resistance and capacitance to reduce channel latency and crosstalk leading to higher bandwidth per channel. When considering the performance of external I/O, impedance matched lines with a reduced number of discontinuities and short channel length are required to improve external I/O performance. Therefore, the electrical design constraints for these signal regimes are vastly different.

High interconnection density, low signal latency, and low signal power all leading to a significant improvement in die-to-die bandwidth per unit power were the main

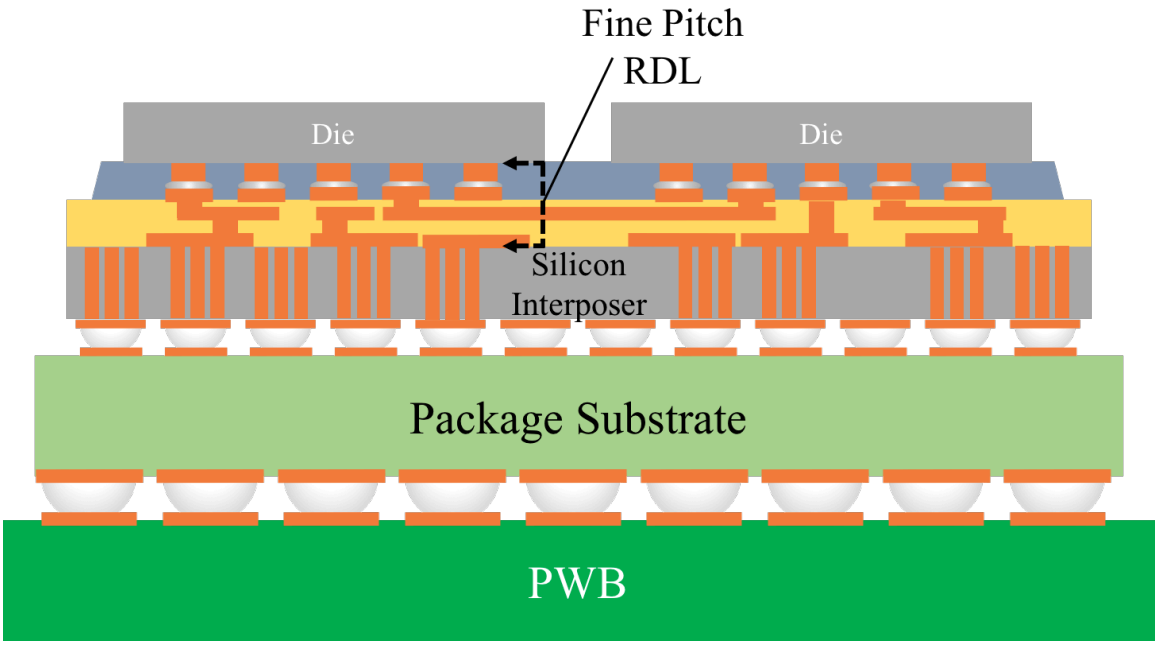


Figure 5. 2.5-D silicon interposer with fine pitch RDL.

advantages of 2.5-D interposers. Future 2.5-D packages, however, must address system level reliability and cost while minimizing the number of interconnect levels to improve external I/O performance.

1.3 Current 2.5-D Interposer Technologies

Aggressive interconnect scaling was required for 2.5-D interposer to achieve interconnect density and performance comparable to or exceeding on-die interconnects. Integration required a tradeoff between bandwidth, fabrication yield, and assembly cost [16]. Yield of a 2.5-D interposer Y_s is the product of logic, memory, and assembly yield such that [17]

$$Y_s = Y_L \cdot Y_M \cdot Y_A \quad (2).$$

The total cost of 2.5-D interposers $C_{2.5D}$ is inversely proportional to interposer yield and directly proportional to assembly cost [17]

$$C_{2.5D} = \frac{\left(1 + \frac{C_A}{100}\right) \times \left(\frac{W_L}{N_L} + \frac{W_D}{N_D}\right)}{Y_S} \quad (3),$$

where C_A is assembly cost in percent, W_L is the logic wafer cost, W_D is the DRAM wafer cost, N_L is the number of logic die per wafer, and N_D is the number of DRAM die per wafer. Scaling CLI pitch required advanced assembly processes including copper pillar with solder cap and copper-to-copper where the correct process was dependent on die size, density, planarity, and yield [8]. RDL scaling required microvia and through-package via pitch to be less than or equal to chip-level bump pitch for optimum die-to-die and die-to-board routing [18]. Therefore, developing 2.5-D interposer technologies required maximizing 2.5-D interposer yield while minimizing cost at acceptable CLI and RDL pitch.

The first 2.5-D interposers implemented in products were based on 300 mm diameter silicon wafers with BEOL dual damascene wiring. Organic interposers were since developed to reduce RDL cost and integrate the interposer and package substrate. Organic laminate thermomechanical properties, however, prevented scaling interconnect density to BEOL silicon interposers dimensions. The following summarize current 2.5-D

interposer technologies and compares them to the 2.5-D glass interposer package to meet packaging requirements for high performance computing applications discussed in 1.1.

1.3.1 Wafer-based Silicon Interposer

The first implementation of a 2.5-D silicon interposer was referred to as stacked silicon integration (SSI) technology shown schematically in Figure 6 to integrate partitioned field programmable gate array (FPGA) devices [5]. Technical and economic challenges including transistor scaling and full reticle die yield respectively prevented a monolithic FPGA implementation from meeting logic capacity, power, and bandwidth requirements. Wafer-based silicon was adopted as a packaging material due to matched CTE and established fabrication process to scale interconnection pitch [19]. Signal power

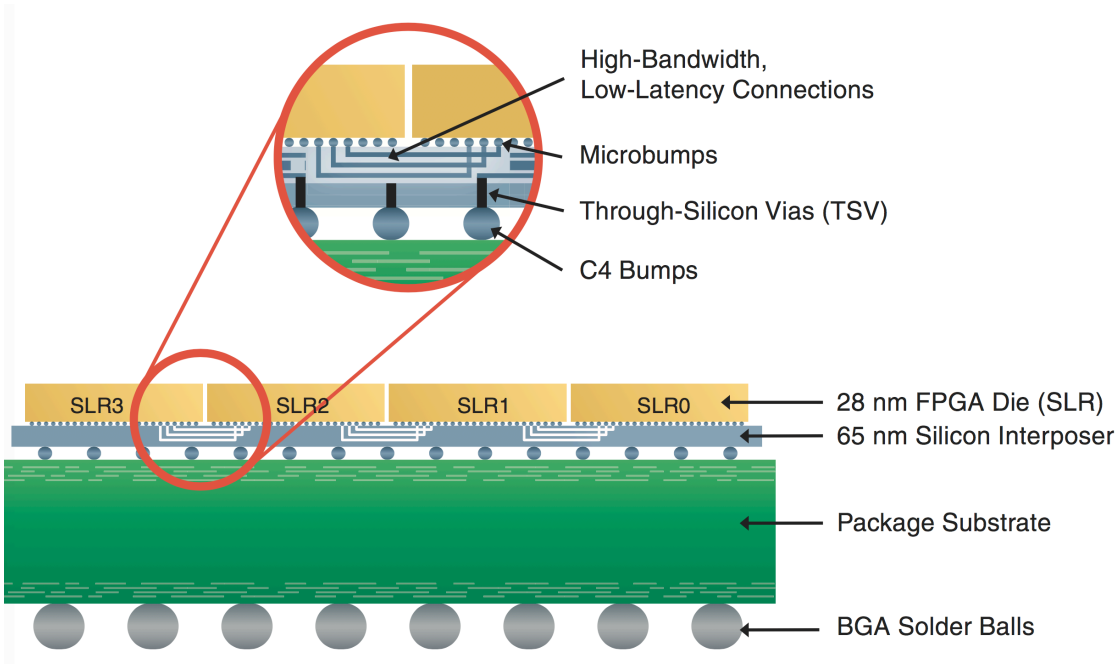


Figure 6. Stacked Silicon Integration technology schematic [5].

was improved by decreasing CLI pitch, latency, and interconnect length while providing up to 10,000 die-to-die interconnections.

The advantage of using a silicon interposer for integration on package was high interconnection density. Interconnection density on silicon interposers was increased by scaling CLI pitch and reducing RDL line pitch and width consistent with 65 nm BEOL design rules. The coefficient of thermal expansion (CTE) of the active die and passive silicon interposer was matched. This improved reliability at bump pitches below 50 μm and provided a roadmap for interconnect density scaling. Side-by-side integration on a silicon interposer provided 20x higher interconnect density compared to organic substrates without power and reliability challenges associated with 3D-IC. Additional advantages of SSI technology included [5]:

1. Reduced latch and signal power by 100x compared to standard I/O.
2. Optimized heterogeneous IC integration.
3. Improved chip-level and ultra-low k dielectric reliability.

Integration of high performance logic with high speed SerDes ICs with added mixed signal noise isolation addressed exterior I/O performance to achieve 25 Gbps that was critical along with wide I/O for HPC system closure. Implementation of SSI using a fully mature, high yield 300 mm silicon wafer processing node improved chip-to-chip stacking interconnection yield up to 99% [6].

The silicon 2.5-D interposer application space has since expanded to integrate a graphics processing unit (GPU) and memory by AMD and NVidia, and will likely include a central processing unit (CPU) and memory by Intel with increased adoption of

HBM [12]. Compared to split logic integration, full reticle and larger-than-reticle interposer size was required to increase memory density and throughput. Cost, limited body size, and high speed performance were the main challenges identified with wafer-based silicon interposers for this expanding application space.

A low cost silicon interposer at 60 µm CLI pitch was proposed to address cost challenges of wafer-based silicon interposers [20]. A semi-additive process (SAP) was used to fabricate RDL to decrease interposer costs. Chip-to-wafer with direct attachment to PWB was used to decrease assembly cost. Line pitch and width at 10 µm and 5 µm, and direct assembly of a 12 mm x 23 mm silicon interposer (66% smaller than full reticle) at 400 µm board-level pitch was demonstrated using these processes.

A double-sided silicon interposer shown in Figure 7 at 40 µm CLI pitch has been proposed to address body size limitations of side-by-side integration on a wafer-based silicon interposer. Implementations of the proposed double-sided silicon interposer

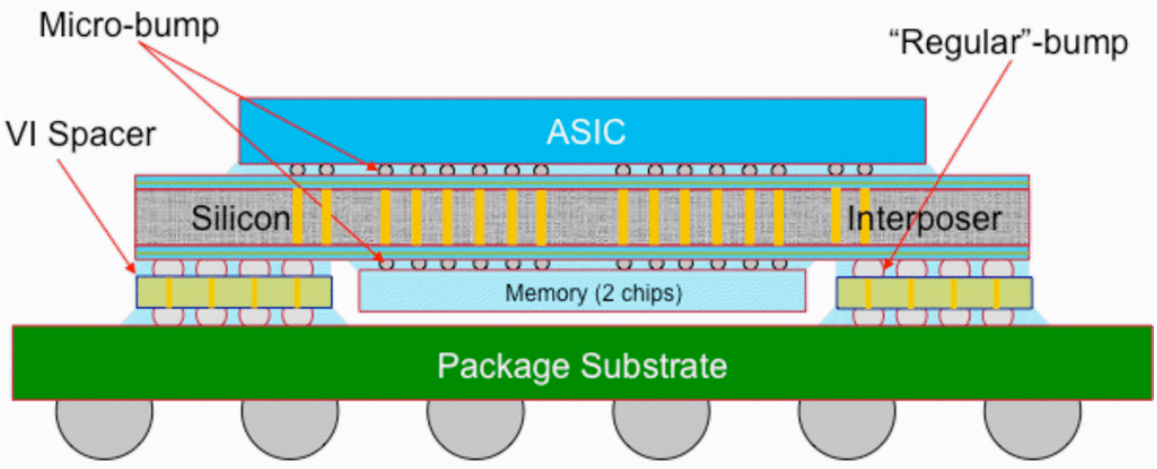


Figure 7. Coarse pitch double-sided silicon interposer [21].

included a foundry process flow (BEOL) and substrate process flow (SAP) using a 300 mm wafer format [4, 21]. These processes are delineated by cost and feature size. The SAP flow demonstrated used 3 μm lithography at 6 μm line pitch and 3 μm copper height, while the foundry process achieved sub-micron line width at 1 μm pitch and 1 μm copper height. A double-sided silicon interposer architecture, however, must consider the effect of TSV and an added packaging layer (vertical interconnect space in Figure 7) on the electrical performance of wide I/O and external I/O respectively.

1.3.2 Panel-based Organic Interposers

The main challenges in silicon interposers becoming a ubiquitous 2.5-D packaging solution were high speed signal performance and cost. Organic packages have been the workhorse of the packaging industry for 30 years. Therefore, scaling conventional organic package substrates was proposed to address electrical loss and cost challenges of silicon interposer while leveraging an existing supply chain and 510 mm x 510 mm panel infrastructure [22, 23]. Two approaches to scale organic substrate interconnect pitch have been pursued: (a) improving organic core materials to scale the RDL line and via sizes using sequential build-up (SBU) processes, and (b) adopting thin film metallization processes to deposit RDL on top of conventional package substrates using modified wafer processes [22, 24].

Key innovations to scale conventional organic substrate interconnect pitch included a low electrical loss ($tan\delta$ = 0.005 at 1 GHz) material set with high modulus (32 GPa) and low CTE (11 ppm/°C) for improved fine pitch reliability. Organic substrates with 12 μm pitch RDL at 6 μm line width and 10 μm copper thickness have been demonstrated with

20 µm blind via on 32 µm via pads using this advanced material set. These design rules led to increased line length and number of routing layers. Consequently, impedance matched wide I/O lines are required. The targeted roadmap for advanced organic substrates included 4 µm pitch RDL with 13 µm microvia on a 22 µm landing pad.

An alternative approach to scaling SBU processes was introduced by integrating thin film RDL on top of a conventional organic substrate as shown in Figure 8 to accommodate 40 µm CLI pitch [24]. Thin film RDL at 2 µm line width were demonstrated using chemical mechanical planarization (CMP) prior to photo-imageable dielectric (PID) deposition by spin coat and SAP with a titanium-copper (Ti-Cu) seed layer. The integration of fine pitch RDL on organic substrate was limited to 21 mm x 15 mm body size (62% decrease compared to full reticle) at a large die-to-die spacing, which increased die-to-die interconnect length.

The main challenges for organic interposer were scaling RDL to match BEOL design rules and reliability at larger than silicon reticle body size.

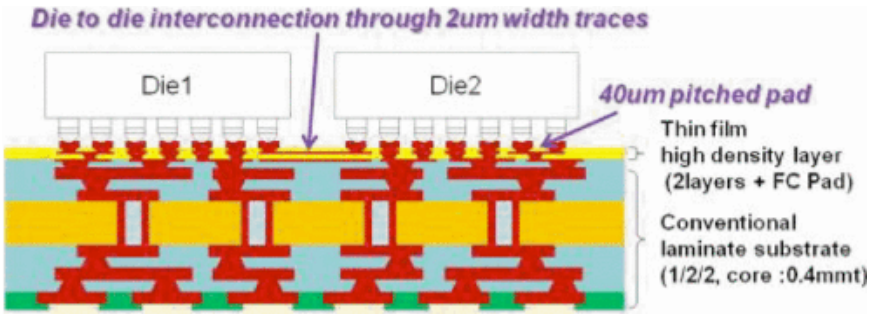


Figure 8. Organic interposer with integrated thin film RDL [24].

1.3.3 Embedded Interposer

Embedded interconnect bridge was an alternative technology recently developed to address performance, cost, and scalability challenges of silicon and organic interposer. Two implementations of this technology included embedded multi-die interconnect bridge (EMIB) and embedded interposer carrier (EIC).

To decrease cost while maintaining die-to-die interconnect density and heterogeneous integration, EMIB was introduced by Intel. This architecture addressed the body size, assembly, and performance challenges associated with SSI. Specific advantages included localized high density interconnects, low cost silicon integration without TSV, and multi-die integration on larger-than-reticle packages [3]. The enabling technology for EMIB was a passive interconnect die fabricated using BEOL RDL, wafer thinning, dicing, and embedding in the top two layers of the package substrate as shown

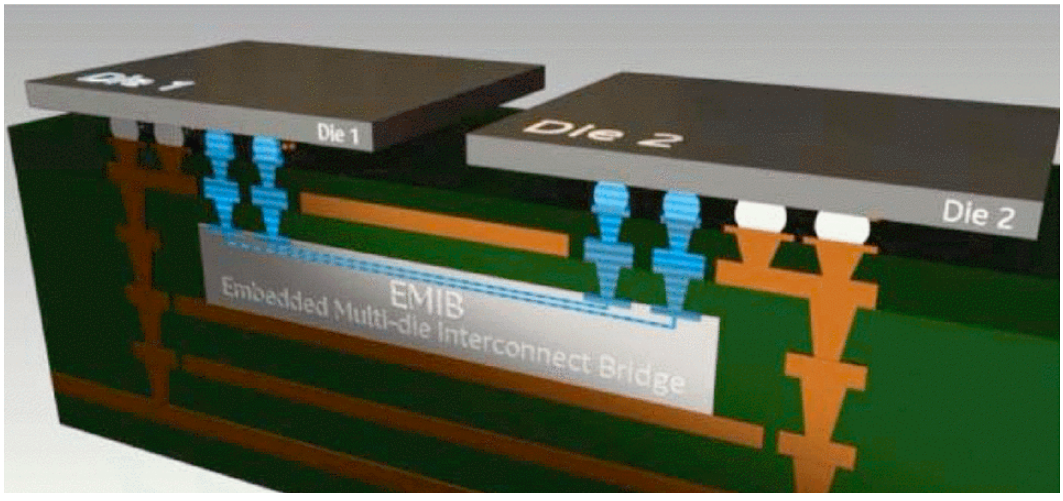


Figure 9. Embedded multi-die interconnect bridge stack-up [25].

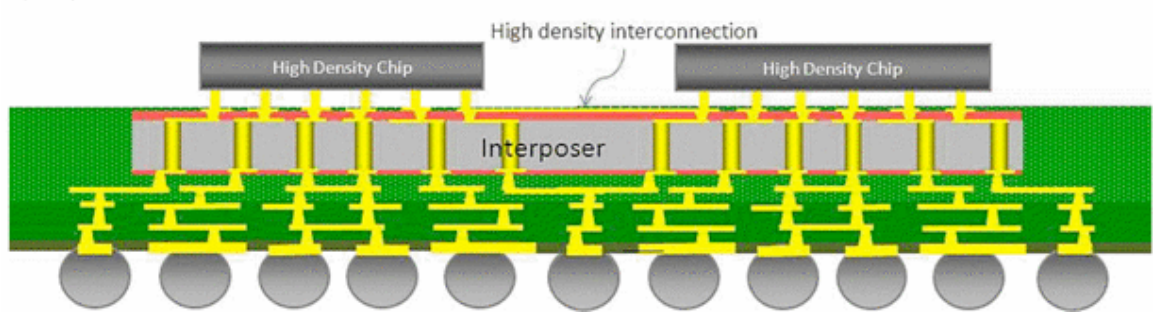


Figure 10. Embedded interposer carrier [15].

in Figure 9.

An embedded glass interposer to achieve 80 µm CLI pitch was proposed to address scalability of organic substrates and complex assembly processes of SSI as shown in Figure 10 [15]. Conventional organic substrates are limited to 20 µm line pitch with 12 µm being demonstrated in research and development [22]. Furthermore, yield losses associated with non-conventional assembly processes including chip-to-chip and chip-to-wafer increase HPC system cost.

Glass interposer, similar to silicon interposer, can be fabricated using wafer processes to leverage a mature toolset and process flow. In particular, through package vias (TPV) were implemented using blind TPV in via-first glass with back grinding after bottom up copper via filling [26]. Redistributive layers were implemented using a Ti-Cu SAP and laser direct imaging to pattern 6 µm pitch RDL [15].

Both embedded architectures integrated localized, high density interconnects for wide I/O within the organic substrate. An added advantage to these approaches was the elimination of a packaging layer and thereby removing added interconnect discontinuities

Table 1. Comparison of 2.5-D interposer technologies.

Packaging Requirement	Silicon SSI [5]	Organic i-THOP [24]	Organic APX [22]	Organic EMIB [3]	Glass Package
Interconnect Density	***Very High*** BEOL	***Medium*** SAP – thin film	***Low/Med.*** SAP – SBU	***High*** BEOL	***High*** SAP
Power	***Med./High*** Conductor Loss	***Med./High*** Long line length	***Med./High*** Long line length	***Med./High*** Conductor Loss	***Low*** Cond. and tanδ loss
Direct assembly to PWB	***No*** Substrate BGA	***Yes*** Integrated BGA	***No*** Substrate BGA	***Yes*** Integrated BGA	***Yes*** Optimized CTE stack
Reliability	***Low*** Substrate	***Medium*** Warpage	***Medium*** Warpage	***Medium*** Warpage	***High*** Glass BGA
Cost	***High*** BEOL wafer	***High*** Single-side process	***High*** High layer count	***High*** BEOL wafer	***Low*** Double-sided Panel process

for die-to-board channels. The main challenge to scaling interconnect pitch beyond current state of the art, however, is assembly tolerances of the embedded die and dimensional stability of the high density package substrate. Interconnect density achieved using EMIB and EIC is ultimately limited by the low dimensional stability and CTE mismatch of the organic substrate and build-up materials. Layer-to-layer registration accuracy is reduced, while warpage due to low elastic modulus limits fine pitch chip-level assembly and reliability.

Current 2.5-D interposer technologies are compared in Table 1 alongside the 2.5-D glass interposer package approach based on the system requirements discussed in 1.1.

1.4 2.5-D Glass Interposer Package

Silicon and organic interposer approaches do not address all the high performance computing packaging requirements described in Section 1.1 for both wide I/O and external I/O signal types and cost. Silicon interposers provide interconnection density and length required for wide I/O, but high speed channels are limited by the electrical properties of silicon. Organic interposers provide low loss high speed channels, but interconnection density is limited by the thermomechanical properties of the organic laminate core.

This research proposes and demonstrates a compelling new 2.5-D glass interposer package approach, combining the high density interconnections of silicon with the low

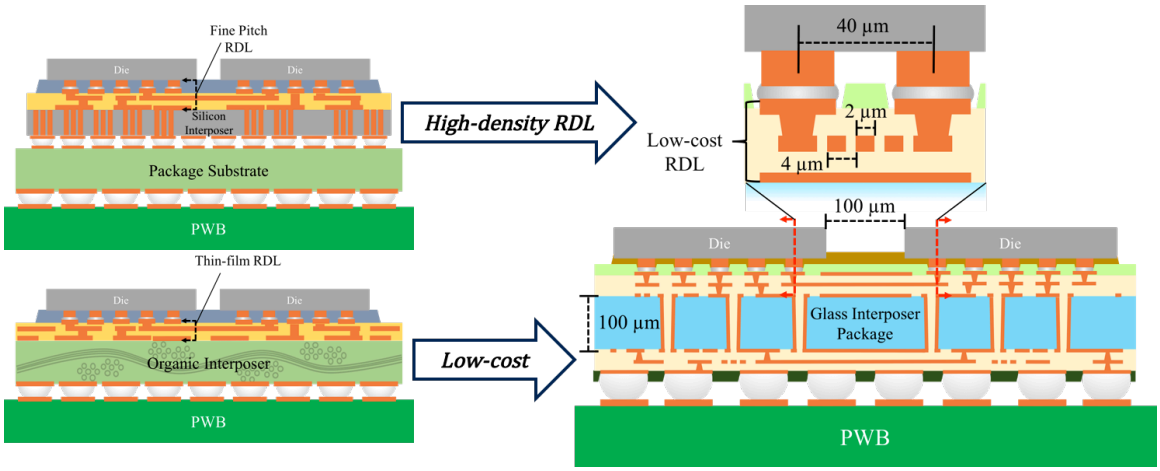


Figure 11. 2.5-D glass interposer package approach for high performance.

loss and large panel processing of organic laminates. A cross-section schematic of a typical 2.5-D glass interposer package is shown in Figure 11, compared to existing silicon and organic interposer approaches.

Salient characteristics of the proposed 2.5-D glass interposer package approach to meet packaging requirements for high performance computing include: fine pitch multilayer RDL wiring to achieve interconnection densities comparable to silicon; thicker signal layer metallization with lower resistance in low loss dielectrics to improve wide I/O performance; direct attachment to PWB to improve external I/O performance; high chip- and board-level reliability as a glass interposer BGA package; and double-sided panel RDL processes to reduce packaging cost.

Glass packaging presents a unique opportunity to optimally scale bandwidth, power, and cost to become the next generation electronic packaging material following ceramics (1970's – '80's) and organics (1990's – 2000's). Smooth surface finish and low total thickness variation of glass enables interconnect line width scaling down to 1 – 2 μm across a 510 mm x 510 mm panel. High modulus and dimensional stability of glass increases interconnect density by scaling via pitch [27]. Lower dielectric constant and loss tangent compared to silicon improves signal speed and power especially for high speed channels that require TPV in the glass core [28]. An optimized CTE stack-up in the package hierarchy from the IC to the system board enables a large BGA glass package [29].

Direct attachment of the 2.5-D interposer to the system board enables a 2.5-D glass interposer package, which provides die-to-die interconnect densities comparable to

silicon wafer BEOL at packaging cost comparable to organic panels. Double-sided and panel-based RDL fabrication processes reduce costs comparable to that of organic substrates in HVM. Furthermore, glass is manufactured by draw processing in thin rolls or panels with low surface roughness, thus eliminating complex back grinding and polishing RDL processes required for silicon BEOL.

1.5 Research Objectives and Challenges

The objective of this research is to model, design, fabricate, and characterize high density, wide I/O and high speed, external interconnections in 2.5-D glass interposer packages for high performance computing applications that require terabit per second bandwidth as shown in Figure 12.

Fundamental challenges that need to be addressed to enable such high bandwidth glass interposer packages are several, and this thesis addresses two major electric design challenges: (a) low latency wide I/O interconnections between ICs on the glass interposer

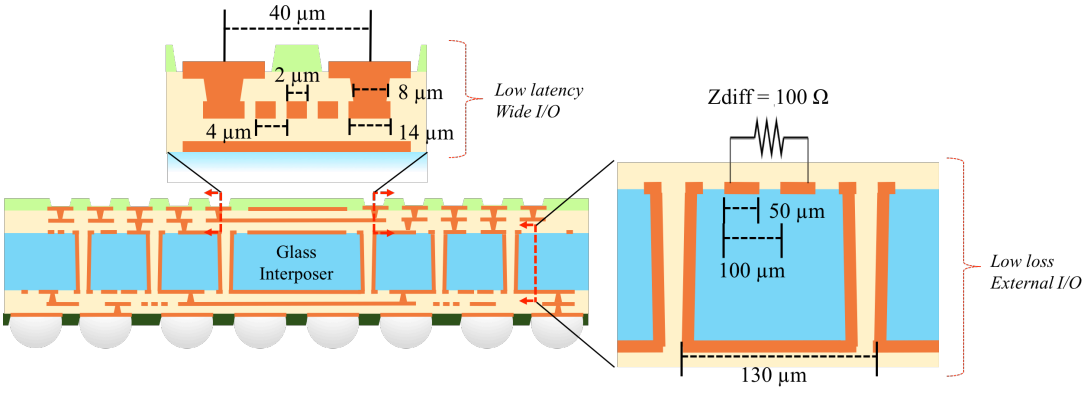


Figure 12. 2.5-D glass interposer with high density and high speed interconnections

and (2) low loss external I/O from the IC to system board. High density interconnections between die require reduced latency (expressed in terms of bit unit interval UI) to improve die-to-die performance at chip-level I/O pitch comparable to silicon interposers. High speed lines require decreased attenuation to improve die-to-board bandwidth. Technical objectives for these signal regimes are compared to the state of the art 2.5-D silicon interposer in Table 2.

Wide I/O interconnection density is dependent on chip-to-package (C2P) bump pitch, RDL microvia padstack diameter, and RDL line pitch and width. An optimized design using these package parameters is required to reduce line latency compared to silicon BEOL by considering parasitic line resistance, capacitance, and inductance. Reducing delay, expressed in terms of bit unit interval (UI) per unit length in Table 2, for wide I/O is critical when benchmarking against existing interposer solutions, which showed a 50% or 1.5 ns increase in delay compared to monolithic integration and system

Table 2. Research objectives and challenges compared to 2.5-D silicon interposer.

Parameter	Objective	Silicon	Challenge
Wide I/O delay	< 0.02 UI/mm (2 Gbps)	0.02 UI/mm (2 Gbps)	Parasitic delay at decreased line pitch and width
External I/O loss	< -0.1 dB/mm (14 GHz)	-0.5 dB/mm (14 GHz)	Crosstalk and losses due to die escape and TGV transition
Chip-to-package pitch	40 µm (C2P)	55 µm (chip-to-chip)	RDL microvia padstack to increase line density at scaled CLI pitch

on chip (SoC) [3]. External I/O loss is dependent on conductor and dielectric losses. Low surface roughness and low dielectric loss tangent reduces these losses for high speed channels. Redistribution layer design at die escape and TPV transitions in the glass core, however, must be considered to minimize impedance mismatch on package in order to maintain overall loss, crosstalk, and timing budgets at increased data rates of 28 Gbps and beyond.

1.6 Research Tasks and Thesis Organization

The research tasks to address the fundamental electrical design challenges summarized in Table 2 that are consistent with the dissertation research objectives to implement high density and high speed interconnections for the 2.5-D glass interposer package architecture include:

Task 1. Modeling and design of high density and low latency RDL for wide I/O between IC.

Task 2. Modeling and design of high speed and low loss RDL for external I/O from the IC to system PWB.

Task 3. Characterization and validation of 2.5-D glass interposer package wide I/O and external I/O RDL technologies.

The basic research results from Tasks 1 – 3 will be leveraged to demonstrate a 2.5-D glass interposer package test vehicle. This test vehicle will demonstrate the integration of low cost, fine pitch RDL and chip-level assembly technologies required for the 2.5-D glass interposer package shown in Figure 11.

The dissertation is organized as follows. This chapter provided the necessary background and motivation for the proposed research objectives, identified the main electrical design challenges to be addressed to achieve these objectives, and described the research tasks to address technical challenges. Chapter 2 summarizes the literature describing the electrical design of 2.5-D interposers to improve wide I/O and external I/O performance. Chapter 3 describes the modeling, design, fabrication and characterization of low latency wide I/O interconnects between die on a glass interposer. Chapter 4 describes the modeling, design, fabrication and characterization of low loss external I/O from the die to the system board. Lastly, the integration of these RDL technologies with a fine pitch chip-level assembly process to show the first demonstration of a 2.5-D glass interposer substrate is discussed in Chapter 5. The research results are summarized and conclusions are discussed in the context of the research objective in Chapter 6.

CHAPTER 2. LITERATURE REVIEW

Integration on package using 2.5-D interposers was necessary to meet future bandwidth requirements of high performance computing systems. Furthermore, 2.5-D interposers dictated two signal regimes—(1) high density, wide I/O and (b) high speed external I/O interconnections with distinct signaling requirements. This chapter summarizes the published literature by others to address the electrical design challenges to implement and improve signal integrity of wide I/O and external I/O in 2.1 and 2.2 respectively.

2.1 Electrical Design of Wide I/O Channels

High bandwidth parallel bus interconnects have been implemented either at the chip- or board-level. On-chip scaling faces challenges from limited conductor cross-sections leading to high resistance in the global interconnect IC layers, resulting in increased latency and limited computing throughput. Packaging ICs individually and connecting them at board-level is severely limited in bandwidth scaling. Large I/O pitch at board-level and long interconnect length result in higher signal power. Microscale package interconnects in 2.5-D interposers provide an optimum balance of I/O density and channel performance to effectively address the chip- and board-level interconnect bottleneck [7]. High density interconnects presented a design advantage for 2.5-D interposers to reduce delay, increase performance, and decrease signal power by shortening interconnect length [16, 17]. In general, the interconnect length (performance) becomes shorter (better) with decreasing interconnect pitch. This was demonstrated using a floating point unit/floating point control benchmark circuit where a 4x reduction in

interconnect pitch from 20 µm to 5 µm decreased the normalized interconnect length by 25% as shown in Figure 13 [16].

The use of wafer-based silicon interposer increased wiring density by 10 – 100x compared to traditional FC-BGA packages, which resulted in 8 – 50x increase in bandwidth compared to standard I/O with a potential 100-1000x signal power reduction [8, 9]. The effect of interconnect length on channel bandwidth, however, was more pronounced for silicon interposers—a 4x increase in line length was found to decrease bandwidth density by 85%—compared to ceramic and organic packages as shown in Figure 14 [10]. Back-end of line silicon interposer technology provided highest die-to-die

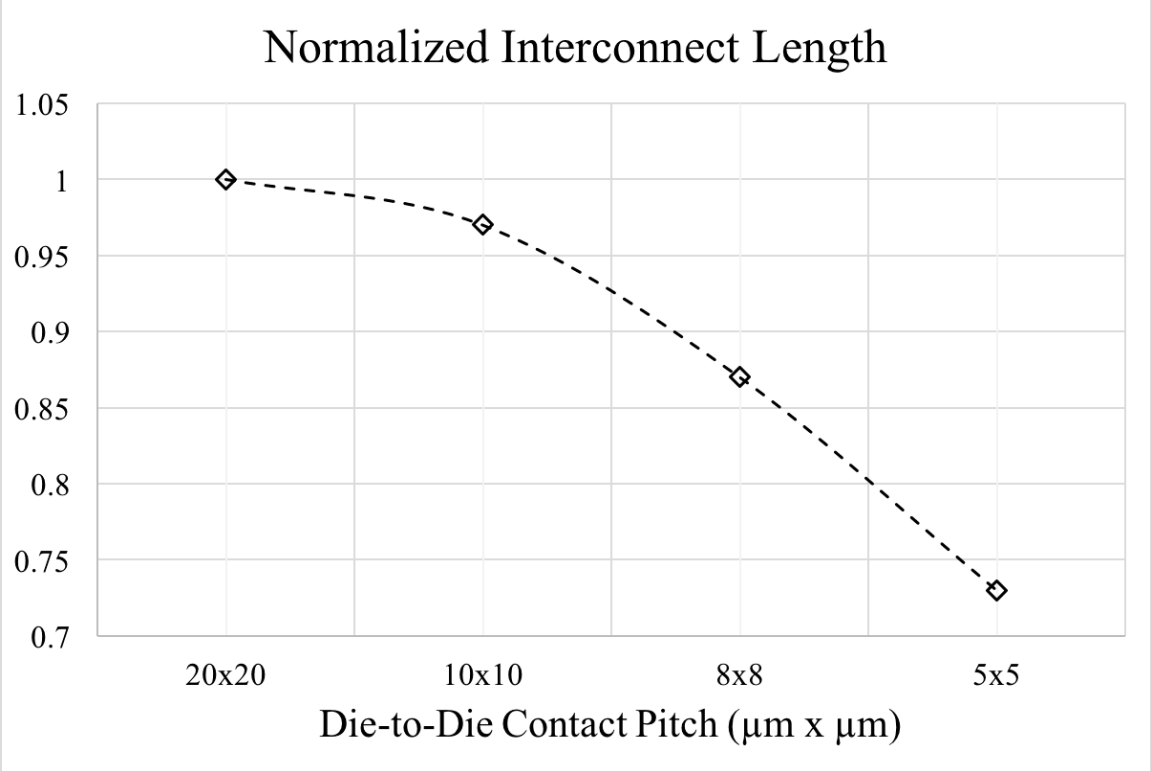


Figure 13. Effect of interconnect pitch on wide I/O channel length [16].

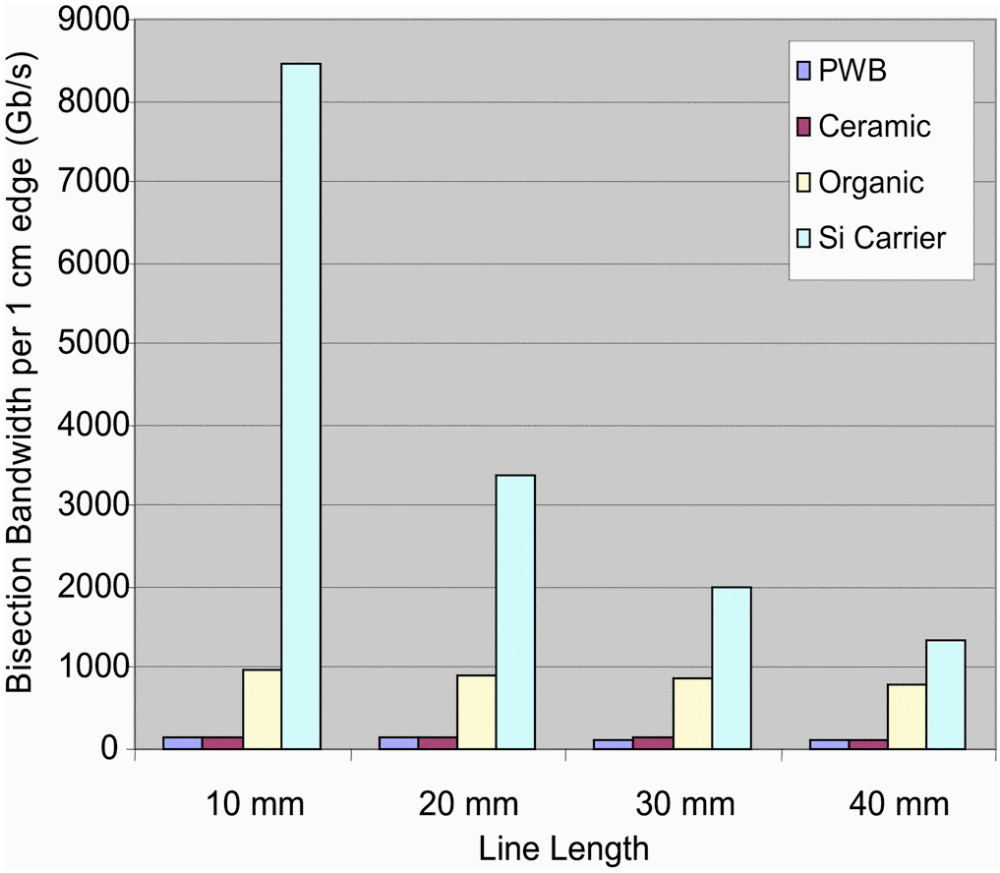


Figure 14. Effect of interconnect length on package bandwidth density [30].

bandwidth compared to existing single chip packaging approaches. The following sub-sections describe the prior art in the design and optimization of the wide I/O interface using BEOL silicon interposers.

2.1.1 Design Process

Silicon interposers used a CMOS buffer to drive wide I/O interconnects [25, 31]. The advantages of using CMOS buffers included: smaller on-chip buffer area, lower sub 1 pJ/bit data transmission, and lower signal speed well matched to existing memory IC

technology. The wide I/O channel was modeled as a general transmission line with G = 0 such that

$$\frac{\partial^2 V}{\partial x^2} = RC\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2} \quad (4),$$

which showed that signal propagation time was dependent on a diffusion component ($RC\frac{\partial V}{\partial t}$) and a wave propagation component ($LC\frac{\partial^2 V}{\partial t^2}$). Signal behavior was dominated by the diffusion component at the frequencies of interest and at line lengths less than 10 mm.

The overdamped response (RC >> LC) had the following implications for wide I/O signaling: no reflections occurred on the interconnect; no overshoot/undershoot occurred during signal transition; and signal rise time was controlled using CMOS buffer size. Therefore, die-to-die interconnects did not require line termination, and the worst-case interconnect performance was modeled using lumped RC elements as shown in Figure 15 [17, 31, 32]. According to this model, C_{Tx} was the output buffer capacitance including on-chip routing, $R_{interposer}$ was the silicon interposer resistance, and $C_{interposer}$ was the silicon interposer capacitance, and C_{Rx} was the input buffer capacitance including on-chip routing. Total on-chip buffer capacitance was approximately C_{Tx} = C_{Rx} = 0.4 pF when considering on-chip routing [32]. Silicon interposer wide I/O exhibited a high resistance—greater than 5 Ω/mm as a result of the 1 μm copper height BEOL design rule and conductivity σ_{BEOL} = 4.2 x 10^7 S/m. Silicon interposer capacitance $C_{interposer}$ was

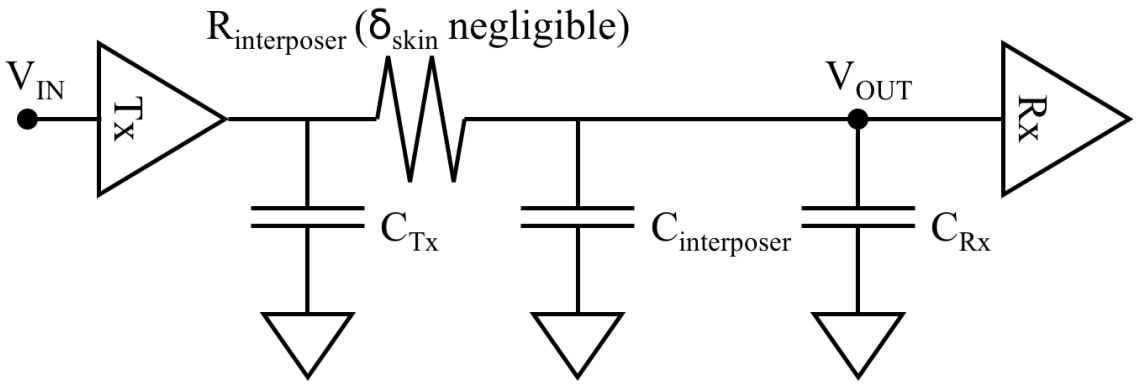


Figure 15. Wide I/O interconnect model [31].

dependent on stack-up and interlayer dielectric (ILD) electrical properties with typical values of $\varepsilon_r = 3.4$ and $tan\delta = 0.01$ [31, 33].

Interconnect bandwidth was inversely proportional to $R_{interposer}$ and total channel capacitance.

$$BW_{Channel} = \frac{1}{2\pi R_{Interposer} C_{Total}} \quad (5),$$

where total interconnect capacitance C_{Total} was

$$C_{Total} = C_{Tx} + C_{Interposer} + C_{Rx} = 0.8\,pF + C_{Interposer} \quad (6).$$

Therefore, the interconnect bandwidth was inversely proportional to the square of the interconnect length L.

The interposer wide I/O design flow shown in Figure 16 was developed based on analyses given in [31-33]. This process flow presents the following design tradeoffs for wide I/O:

1. Interconnect length vs. bandwidth assuming:
    a. G = 0 S/m
    b. RC >> LC
2. Capacitance vs. crosstalk vs. line density.
3. Routing layers vs. dielectric stack-up vs. line spacing.
4. Minimum rise time vs. signal integrity vs. power integrity.

The silicon interposer behaved as a two-pole RC filter (given assumptions 1a. and 1b.) that imposed a cutoff frequency. This cutoff frequency was dependent on channel capacitance and resistance and inversely proportional to the square of the signal length. This presented a trade off in channel capacitance. To reduce capacitance, dielectric

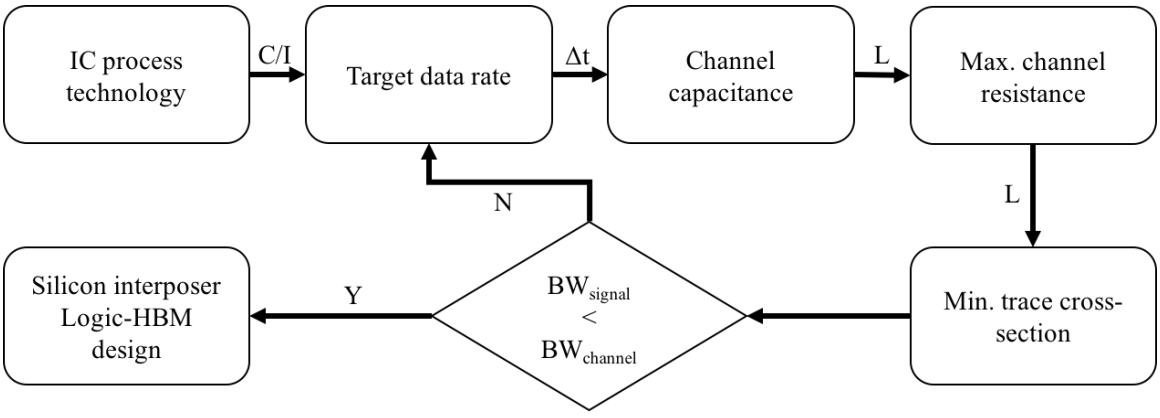


Figure 16. Interposer wide I/O design flow.

thickness was increased, but this reduced coupling to the signal return path, which, in turn, increased crosstalk. Therefore, bandwidth is ultimately dependent on the interposer stack-up with key metrics listed in design tradeoff 3—routing layers, dielectric stack-up, and. line spacing.

When BW_{signal} was less than $BW_{Channel,}$, there was no edge distortion imposed on the rising or falling edge, full swing occurred at the receiver with no inter-symbol interference (ISI), and no equalization was required [31]. Therefore, the signal rise time (not the signal data rate) determined the target bandwidth of the silicon interposer interconnect. In general, the signal rise time decreased at higher data rates. The minimum rise time achieved by a CMOS driver was dependent on the *C/I* process parameter:

$$\Delta t_{min} = \Delta V \frac{C_{Device}}{I_{Saturation}} \tag{7}.$$

The BW_{signal} was computed using the rise time bandwidth approximation based on the 30 – 70% signal rise time of the circuit shown in Figure 15 with an RC time constant τ.

$$BW_{Signal} = \frac{1}{2\pi\tau} = \frac{\ln\left(\frac{1-0.3}{1-0.7}\right)}{2\pi\Delta t} \tag{8}.$$

Wide I/O performance was limited to 2 Gbps using a CMOS buffer sized to achieve I_{sat} = 20 mA and drive a L = 6 mm line based on the design process flow given in Figure 16. Simulation of wide I/O channels using BEOL RDL and C_{device} = 0.4 pF indicated a tradeoff between data rate and channel length, but ultimately showed that

BEOL design rules limited data rates at channel lengths L > 10 mm. This is mainly due to large line resistance and decreased swing at the receiver [25].

Lastly, based on silicon interposer design rules, the minimum rise time required to achieve the targeted data rate required a tradeoff in signal integrity and power integrity. If the rise time was reduced to meet channel data rate, a decreased parasitic inductance was required for the PDN given the increase in I_{Sat} during switching events. The silicon interposer design process summarized in Figure 16 considered an ideal case. Typical timing budget for signaling included 0.2 UI for signal rise time. Additional eye closure occurred due to PDN-induced jitter and crosstalk between wide I/O lines. The effect of voltage variation on CMOS gate delay is given in Figure 17, and a 50 mV differential budget was recommended for crosstalk to meet wide I/O timing budget [32].

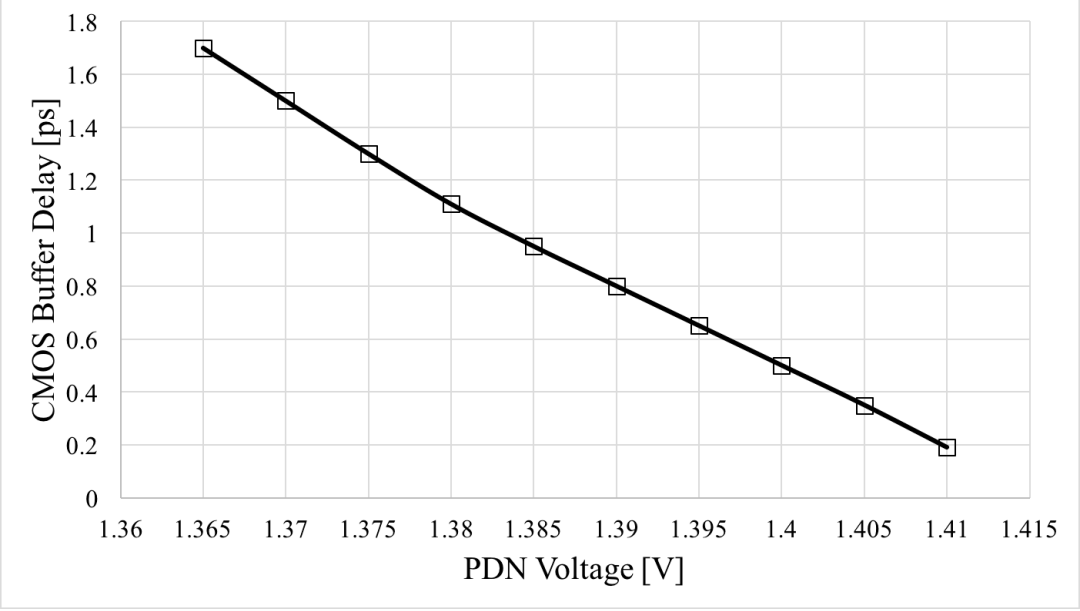


Figure 17. Voltage dependent CMOS buffer delay [32].

Wide I/O signal power was dependent on activity factor α, total channel capacitance C_{Total}, swing voltage V, and clock frequency f (half the data rate) such that [25]:

$$P = \alpha C_{Total} V^2 f \quad (9).$$

Equation 6 assumed the channel was modeled as an RC circuit similar to the model shown Figure 15. The activity factor was $\alpha = 0.5$ for random data. Data bus inversion was used to improve signal power by reducing $\alpha = 0.4$.

The design process for a silicon interposer using CMOS buffers showed that signal rise time was controlled by driver sizing and was fundamentally limited by driver capacitance, which depended on the *C/I* silicon process parameter. Furthermore, the signal edge characteristics at the CMOS receiver was limited by the BEOL interconnect resistance and capacitance that determined the wide I/O channel bandwidth. Wide I/O data rate for a BEOL, wafer-based silicon interposer was therefore limited by minimum rise time that the interconnect supported, and increasing data rate required decreased resistance, capacitance, and channel length.

2.1.2 Design Optimization

High interconnection density was achieved on silicon interposers, but fine pitch BEOL RDL and increased activity factor affected the signal integrity of this interface. Wide I/O design rules and stack-up were limited by CMP as shown in Figure 18. Copper height was typically 1 μm [6]. Inter-layer dielectric thickness was approximately half the

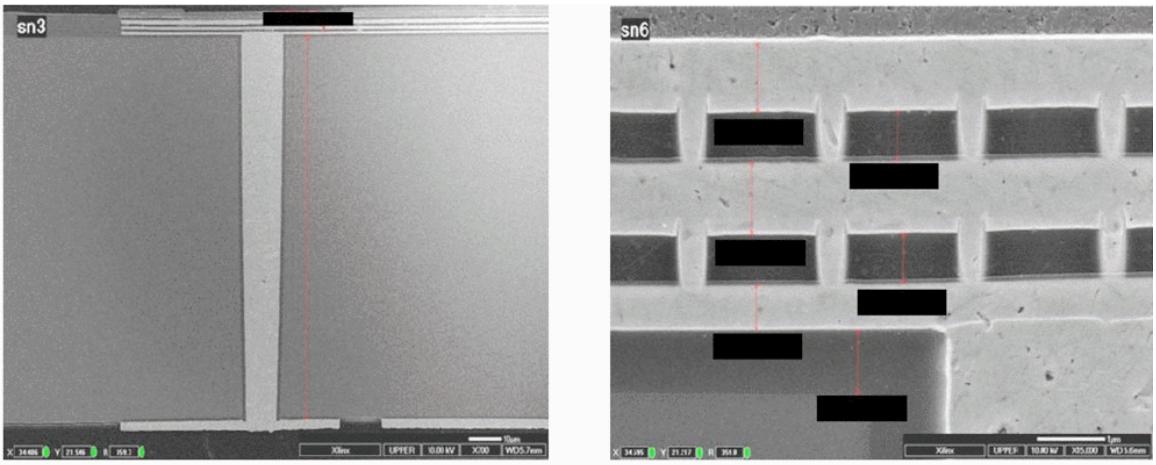


Figure 18. Wafer-based silicon interposer stack-up [6].

copper height [34]. Solid reference planes were not allowed, and grid or mesh planes with a maximum 65% – 75% copper coverage were required for reference layers [35]. Therefore, challenges for signal integrity, based on these fabrication constraints, included high line resistance and capacitance and high dielectric losses with increased coupling to the silicon substrate.

Conductor loss less than -2 dB was typical of silicon interposer channels at low frequencies due to the design rule limitation of damascene processes. The increased activity factor posed additional electrical design challenges including channel loss and delay due to simultaneous switching noise and crosstalk [11, 34, 36, 37]. Design techniques to improve signal integrity of silicon interposer wide I/O include trade-off analysis of line width and space and line length, as well as stack-up improvements discussed below.

2.1.2.1 Line Pitch, Width, Length

Wafer-based silicon interposer design rules resulted in high insertion loss and crosstalk for wide I/O. Trade-off analyses to improve line loss and crosstalk were performed [38]. The result of this study demonstrated that wide I/O line pitch and width must be optimized for signal integrity by considering the following factors:

1. Line density based on line pitch and width.
2. Increased line spacing reduced crosstalk.
3. Increased line width reduced insertion losses (especially below 1 GHz).

Increased line width and space improved signal integrity but at the cost of decreased line density. Decreased channel density led to increased line length, which must be less than 5 mm— the critical path length for silicon interposer. Additional approaches to decrease crosstalk of die-to-die interconnects included adding guard traces with ground vias to reduce crosstalk induced jitter and voltage over/under shoot [37]. This method, however, increased wide I/O routing area compared to simply increasing the line spacing (where $S = 3W$ was found to be most effective design trade-off).

Time domain analysis for wide I/O crosstalk was performed using guard traces between signal traces [36]. This study considered the crosstalk between die-to-die interconnects for unidirectional and bidirectional signaling. The effect of capacitive and inductive coupling on crosstalk varied with the signal topology. This was attributed to the lack of matching termination used for wide I/O as shown for the unidirectional signal topology in Figure 19. The victim line was tied to VDD for this analysis. Therefore, the

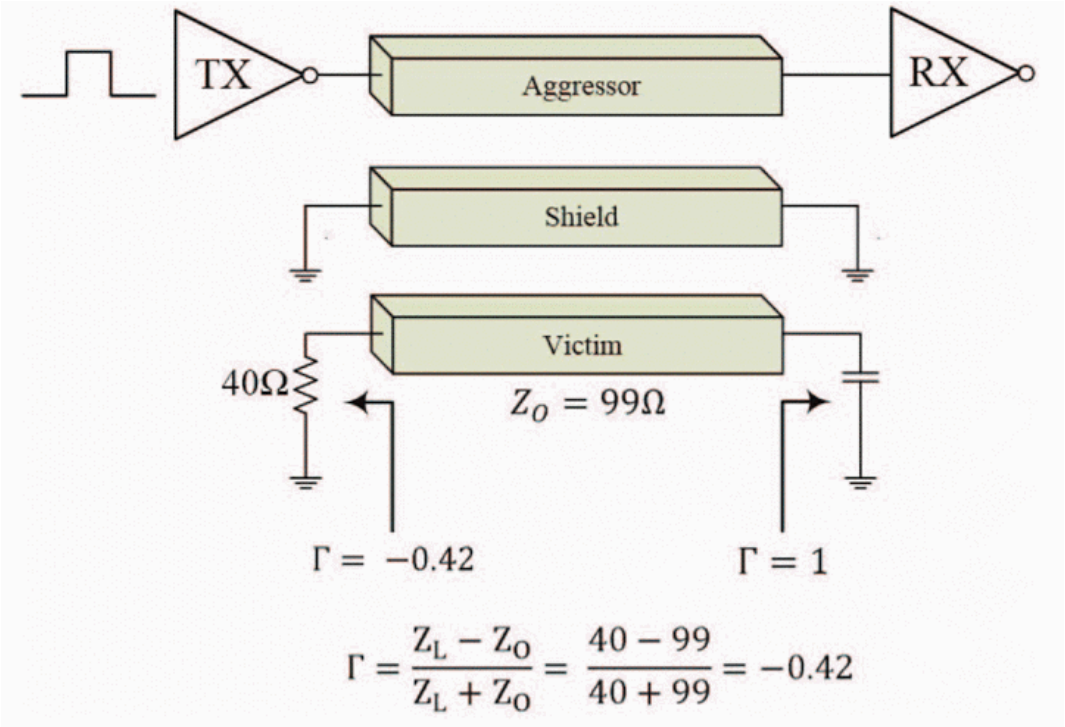


Figure 19. Wide I/O crosstalk analysis for SSI [36].

termination to ground was through the NMOS transistor device, while the receiver termination was considered open due to on-chip routing and gate capacitance.

The simulated crosstalk for the unidirectional topology is shown in Figure 20. Near-end crosstalk is the sum of voltage noise arising from capacitive and inductive coupling. Far-end crosstalk changed based on current flow. Initially, voltage noise from capacitive and inductive coupling cancelled each other, and the voltage noise was due to reflections at the receiver. Then, as the aggressor transistor began to turn off, voltage noise at the far-end was the sum of capacitive and inductive coupling due to a change in current polarity.

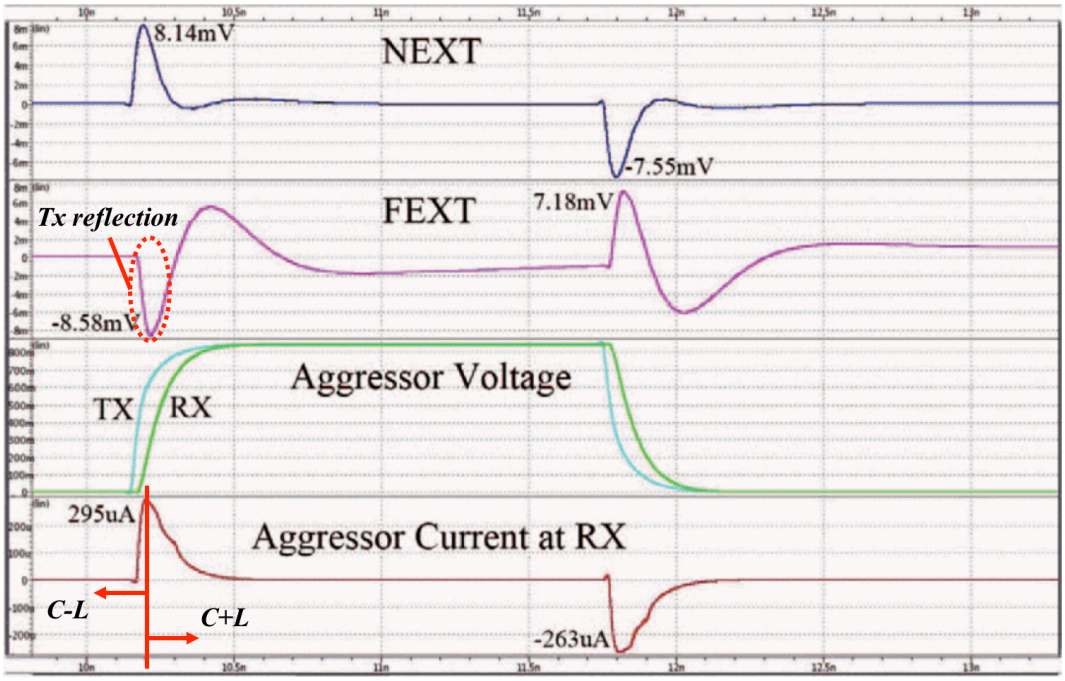


Figure 20. Crosstalk for unidirectional signal topology and ground shielding [36].

2.1.2.2 Stack-up

The effect of signal layer assignment on die-to-die insertion loss was studied and the stack-up analyzed is shown in Figure 21 [39]. The silicon interposer used a six-metal layer stack-up with 1 µm ILD and copper thicknesses to implement microstrip line and stripline transmission line structures.

Conductor loss dominated insertion loss below 1 GHz for each type of transmission line structure. Increased capacitive loading for the stripline structure increased losses above 1 GHz relative to the microstrip line, while the M5 stripline line showed highest insertion loss due to increased coupling to the silicon substrate. This was mainly due to the mesh reference layer on M6. Simulated statistical eye diagrams using these

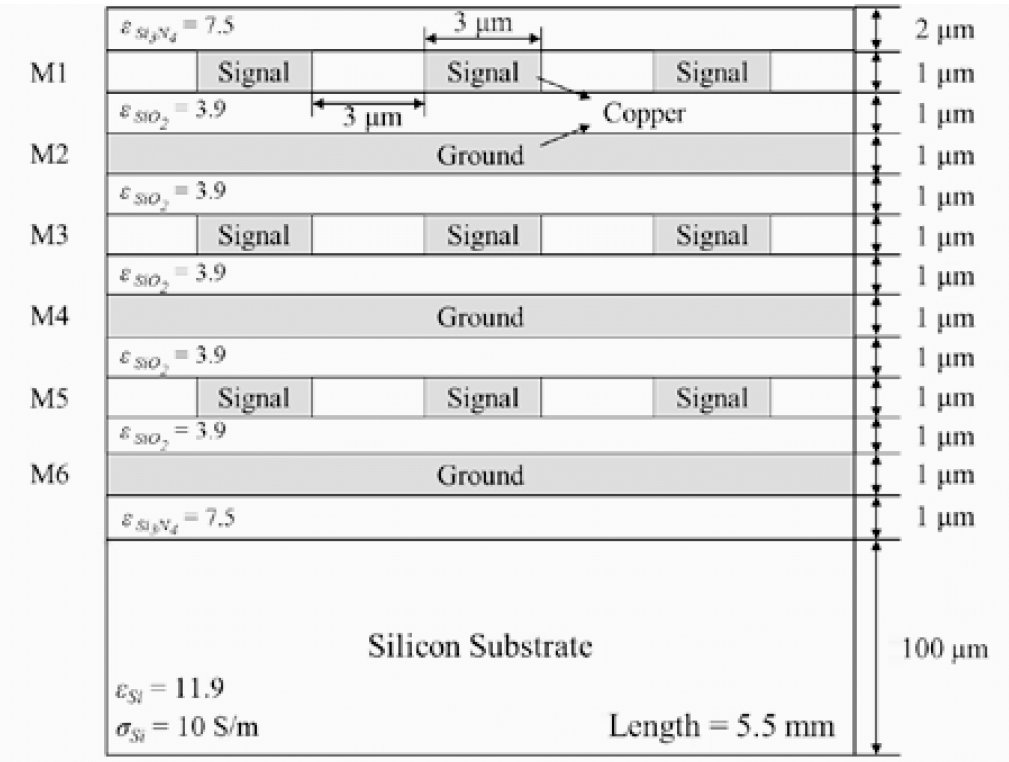


Figure 21. Silicon interposer wide I/O stack-up [39].

transmission line structures showed the capacitive loading and substrate coupling resulted in added jitter compared to the microstrip line.

A trade-off study comparing crosstalk and crosstalk induced jitter for different interposer stack-ups shown in Figure 22 was performed [36]. Crosstalk analysis showed that inductive coupling dominated capacitive coupling in test cases 1 – 3. This was attributed to the increased number of guard traces on all four sides of the victim line (shown in red in Figure 22). Furthermore, inductive coupling was shown to be largely independent of line spacing and directly dependent on the number of aggressors. Capacitive and inductive coupling were significant for cases 4 – 6 where the number of guard traces was reduced. Inductive coupling tended to dominate capacitive coupling

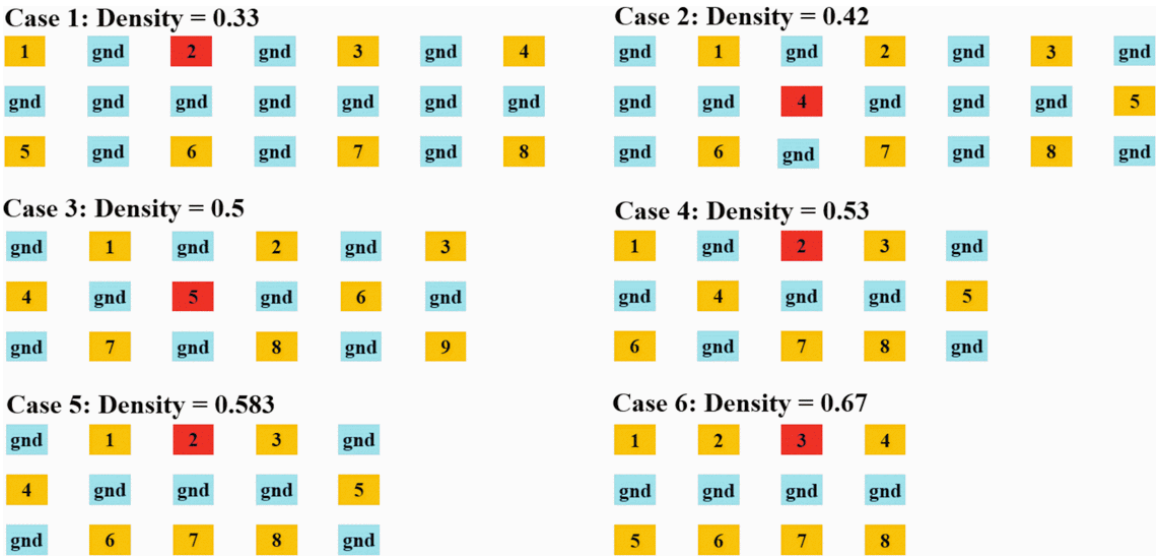


Figure 22. Silicon interposer stack-up crosstalk trade study [36].

depending on the number of aggressors. In general, peak crosstalk and crosstalk induced jitter increased with signal density where signal density was defined as:

$$signal\ density = \frac{signal\ lines}{total\ traces} \quad (10).$$

2.1.3 Emerging High speed Wide I/O

Future bandwidth roadmaps call for higher die-to-die data rates. This trend was demonstrated in the latest specifications for HBM where line rates increased from 1 Gbps to 2 Gbps [13]. This had three major effects on the wide I/O design: (a) decreased channel losses were required to maintain signal power budget; (b) parasitic resistance and capacitance for on-chip routing between TSV and I/O bump had a major effect on 2.5D

signaling; and (c) equalization and the effect of TSV became prominent in achieving increased data rate.

The silicon interposer stack-up was modified to reduce frequency dependent coupling to the silicon substrate [34]. The current flow for transmission lines, which referenced non-intrinsic silicon, changed with frequency and doping concentration. Field analysis was used to show that the silicon interposer behaved as a conductor at low frequencies and as an insulator at higher frequencies. This resulted in increased dispersion and inter-symbol interference. The layer assignment for a four-metal layer silicon interposer stack-up was modified to improve ISI-induced jitter as shown in Figure 23. The top layer of the silicon interposer was reserved for aluminum under bump

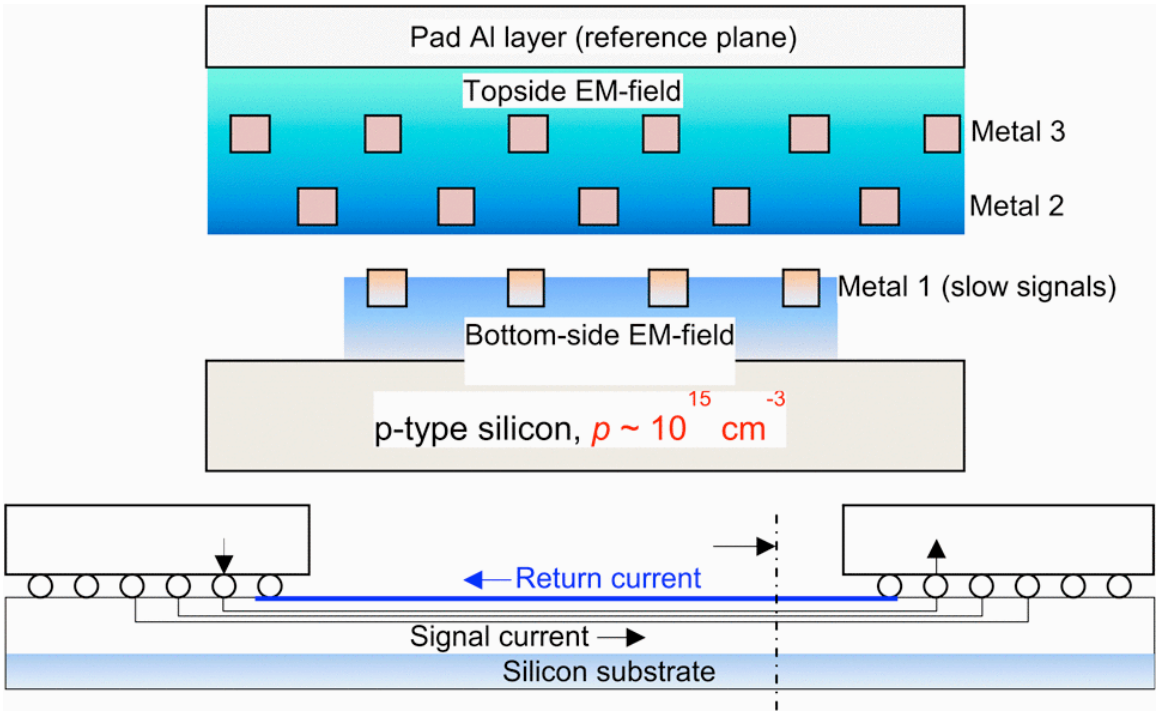


Figure 23. Signal layer assignment for wide I/O [34].

metallurgy (UBM) and did not require CMP. Therefore, a solid reference plane was available to improve signal integrity. Interior metal layers closer to the silicon substrate were reserved for lower data rate channels less sensitive to signal dispersion.

Decreased wire cross section increased loss of silicon interposer interconnects. Modified BEOL stack-ups were introduced, as shown in Figure 24, to improve channel performance. Insertion loss was reduced by using thicker and wider copper traces or thicker oxide layers to reduce line resistance and capacitance respectively [40]. Increased

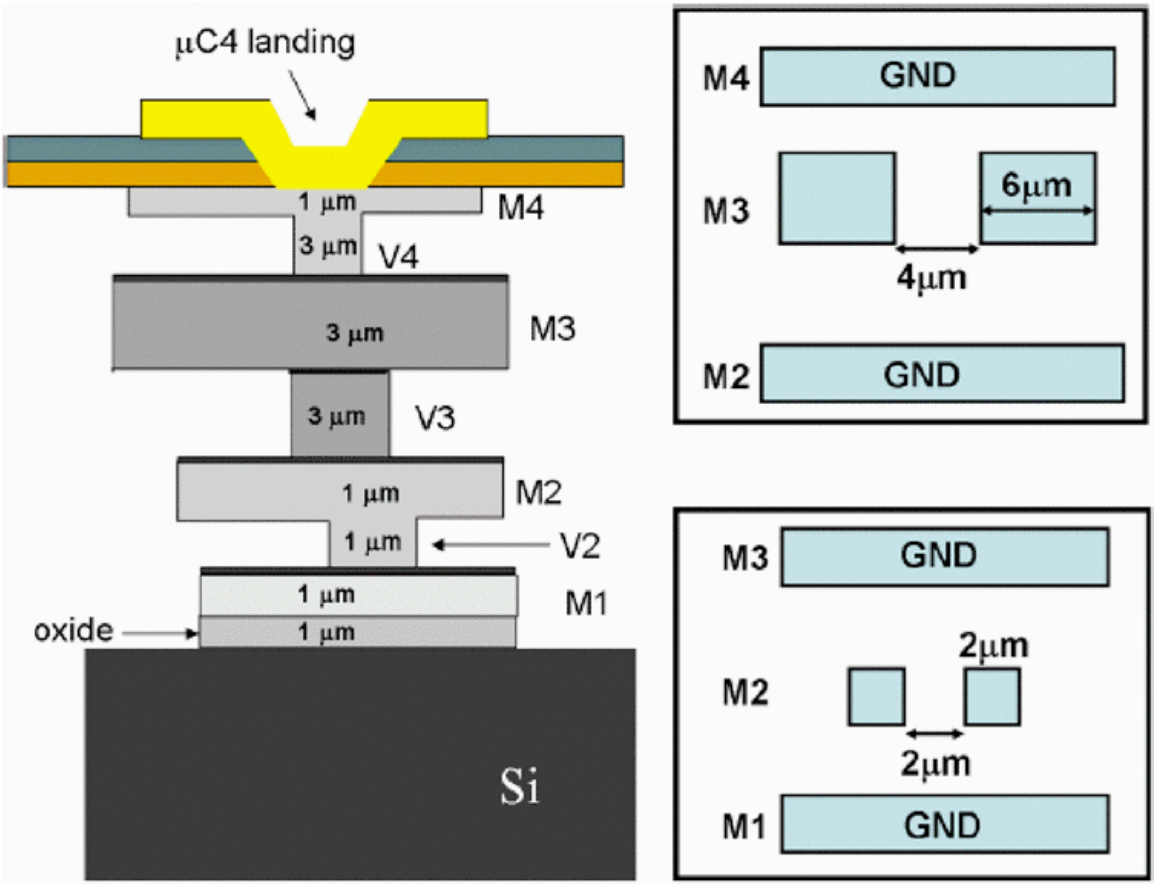


Figure 24. Stack-up for high speed die-to-die interconnects [40].

wide I/O data rates presented a tradeoff between line density and line speed since resistance tended to dominate losses.

Maximum line density was ultimately fixed based on line resistance and higher data rate per channel wide I/O signaling will become necessary for split logic and logic and memory integration. Increased data rate was demonstrated using passive equalization on silicon interposer [41]. Active equalization techniques used for external I/O are not feasible for wide I/O due to power and on-chip overhead [42]. Implementation of the passive equalization was realized using structures embedded within the ground plane. Passive equalization techniques assumed sufficient signal power which dictated a tradeoff between maximum data rate and signal power. Increased wide I/O data rate also required careful clocking and pipelining design. Added complexities to clock distribution included core and signal domain clocks to improve signal jitter tolerance, as well as clock groups to improve wide I/O routing constraints. Furthermore, high speed wide I/O required silicon overhead to implement tunable on-die terminations, decoupling, and electrostatic discharge [18].

2.2 Electrical Design of External I/O

High speed channels from the 2.5-D interposer to other system components are required for HPC design closure [5]. Silicon interposers provided the highest interconnect density for wide I/O interfaces, but faced several electrical design challenges for die-to-board channels that included a TSV in the high speed data path.

Insertion losses up to -0.9 dB at 20 GHz were attributed to the TSV as shown in Figure 25 [43]. Therefore, high speed channels required optimization of TSV design

parameters as well as interposer, substrate, and board electrical co-design to maintain channel loss and timing budgets. The external I/O data path included CLI bump, topside BEOL RDL, TSV, and bottom side RDL/UBM routing. The main design challenges for silicon interposer included TSV capacitive loading, TSV crosstalk, and RDL/UBM-to-silicon coupling [6]. Addressing these challenges was required to improve insertion loss

Topside RDL insertion losses were improved by decreasing coupling to the silicon substrate [43]. High speed lines used a three-metal layer stack-up fabricated using wafer-based silicon processes including copper damanscene as shown in Figure 26. The top-most layer was reserved for high speed signaling with the two underlying metal layers

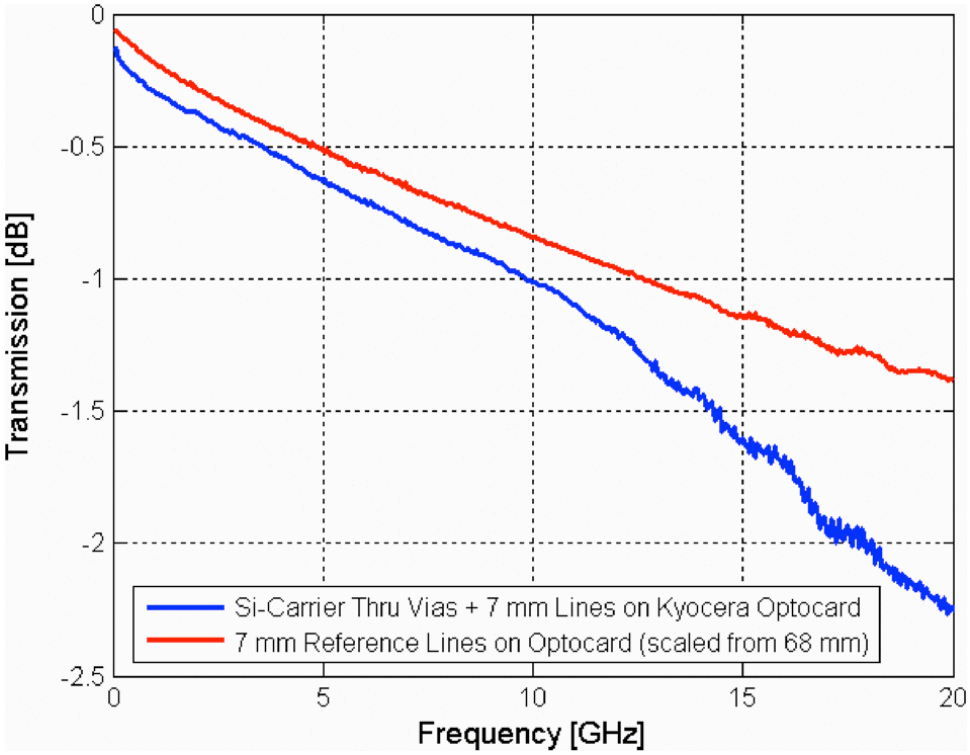


Figure 25. Effect of TSV loss on channel budget [43].

reserved for reference layers. A -0.43 dB/mm attenuation was achieved using differential microstrip lines implemented using this stack-up on a silicon carrier.

Through silicon via capacitance depended on wafer resistivity and silicon bias. The frequency dependent capacitance caused high insertion loss at low frequency [19]. Capacitive loading of TSV was decreased using high resistivity (20 Ω·cm) silicon. High resistivity silicon was not compatible with devices for applications that required an active interposer, which were limited to 8-12 Ω·cm. The effect of wafer resistivity and bias is shown in Figure 27. The metal-oxide-semiconductor capacitance was considered for

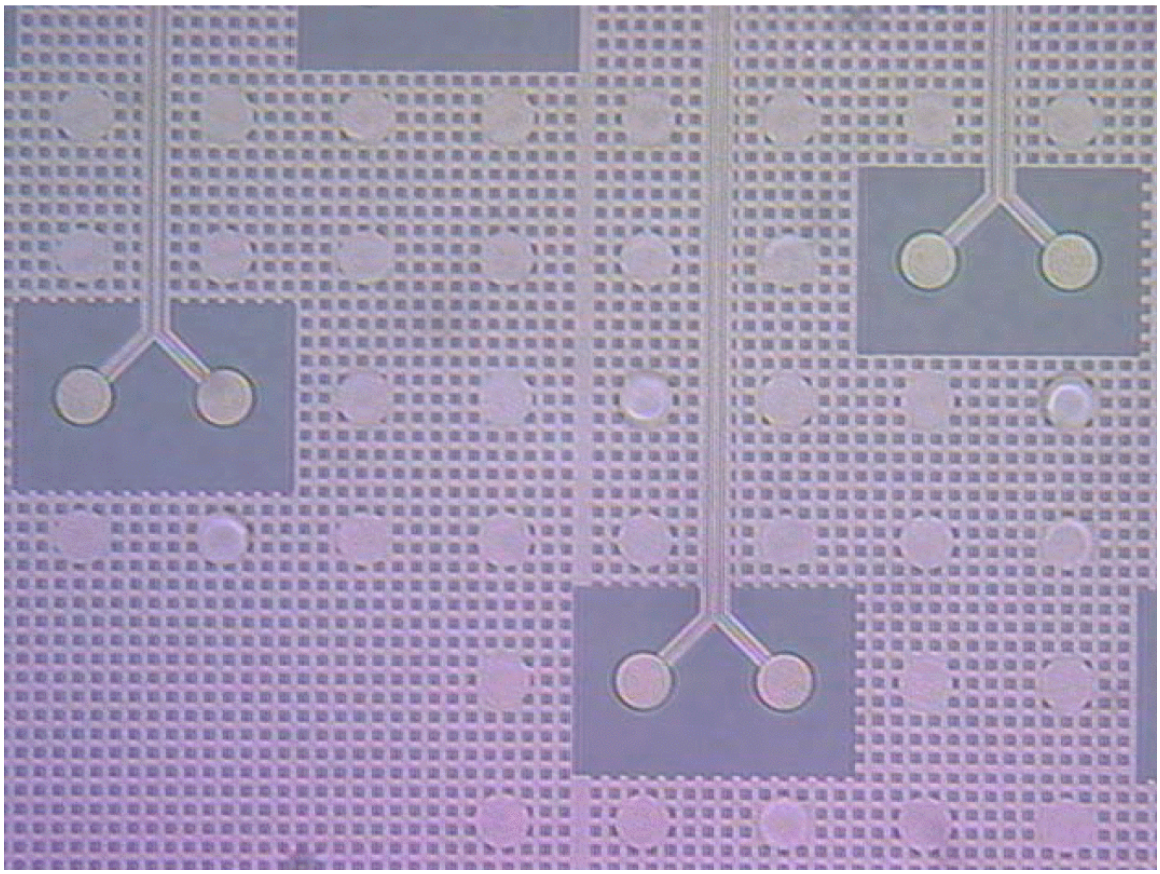


Figure 26. External I/O topside RDL stack- up [43].

active interposers. This capacitance was in series with the oxide capacitance and lowered the TSV capacitance at low frequencies.

Silicon interposers used a thin inter-layer dielectric, primarily due to CMP design rule limits. This affected the signal integrity of back-side RDL layers where a coplanar waveguide (CPW) structure was used for signal routing from the TSV to the C4 bump [44]. The backside RDL layer typically used a silicon nitride ($\varepsilon_r \approx 8.0$) dielectric [33]. This increased capacitive loading (directly dependent on ε_r) and delay (directly dependent on square root ε_r). A thicker backside ILD up to 7 µm was used to improve insertion loss as shown in Figure 28.

High resistivity silicon decreased effective TSV capacitive loading leading to 2x lower insertion loss at 14 GHz [45]. Increasing silicon resistivity to 20 $\Omega \cdot$cm reduced loss, but was not compatible with active silicon interposer design [6]. High resistivity active silicon has gained traction with the progression of RF-CMOS, as well as silicon on insulator to improve UBM RDL line loss by roughly 2x [44]. Therefore, the main

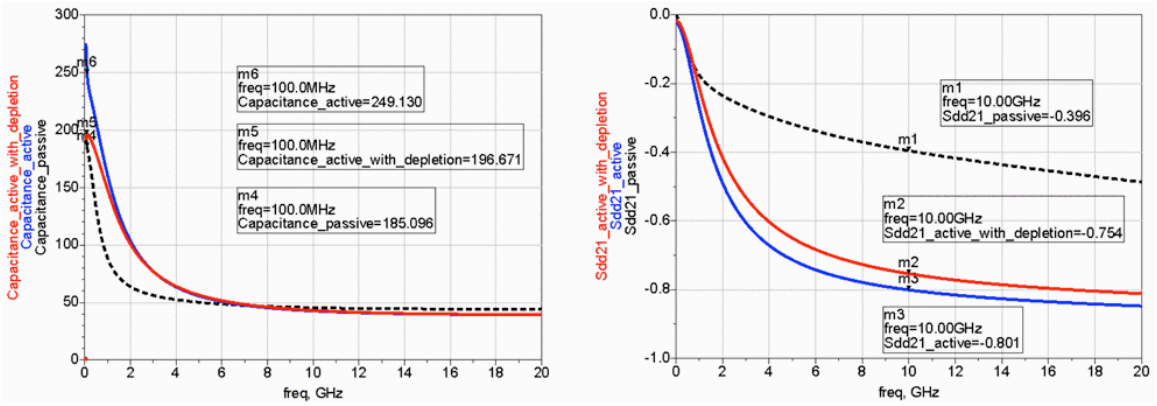


Figure 27. Effect of silicon resistivity on TSV capacitance and loss [6].

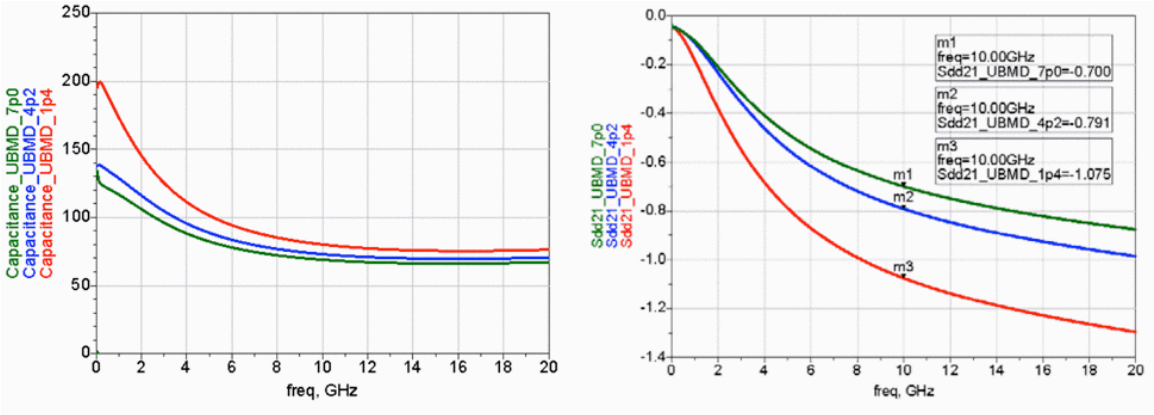


Figure 28. Effect of interlayer dielectric thickness on external I/O loss [6].

limitation to improve silicon external I/O performance was dielectric thickness. Step coverage for high aspect ratio TSV, thermal oxide growth rate, and thin film stress limit the maximum oxide thickness for silicon interposer between 1 – 3 um [6, 44].

The effect of wafer resistivity and bias, as well as ILD thickness on external I/O performance was compared in Figure 29 using time domain analysis [6]. Added signal length and loss due to silicon interposer degraded the eye opening from 0.43 UI @ 1E-12 to 0.32 UI @ 1E-12 at 13 Gbps. Thicker ILD layers improved the eye opening by up to 18%, while thicker depletion capacitance improved eye opening by up to 9%. Both ILD thickness and depletion capacitance, however, did not improve opening above 0.40 UI. At 28 Gbps line rate TSV loss became significant and equalization was required [14].

Substrate electrical co-design to meet signal requirements was required for silicon interposers [14]. Interposer substrate figures of merit included dielectric loss, skin effect, and surface roughness. Silicon interposer required a low CTE organic or low temperature co-fired ceramic (LTCC) substrate to manage thermomechanical stresses at the second

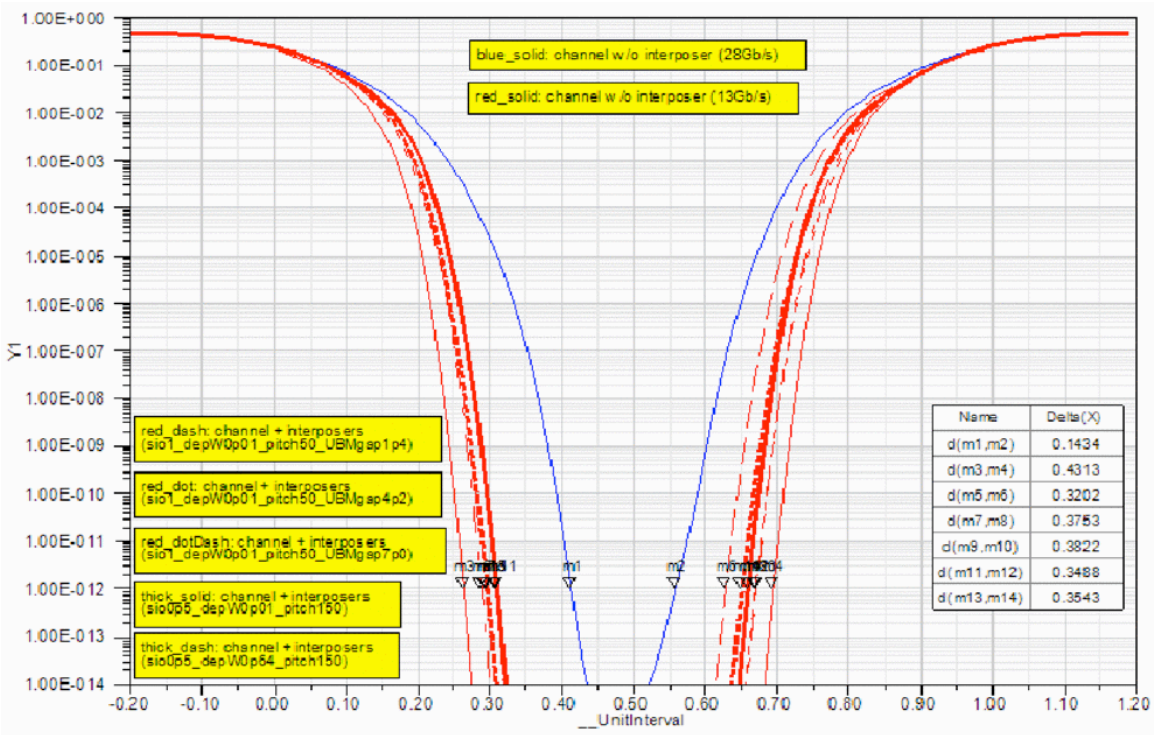


Figure 29. Interposer + LTCC + PWB bathtub curve 13 Gbps and 28 Gbps [6].

level interconnect solder bump. Larger interconnect cross section and lower copper surface roughness using LTCC reduced conductor losses. Non-uniform signal transmission in the core material was the main drawback for organic substrates. Channels on LTCC outperformed organic substrates by approximately 2x with respect to insertion loss. The thick LTCC stack-up required added on-interposer or on-chip decoupling capacitance. Silicon interposer allowed for trench capacitors to reduce on-chip decoupling overhead. The added interconnect between the interposer and substrate required improved pad design to reduce the effect of this impedance discontinuity. After interposer assembly, C4 collapse increased coupling to adjacent pad ground planes. This was improved by increasing ground anti-pad near signal C4 bumps.

Glass *Organic*

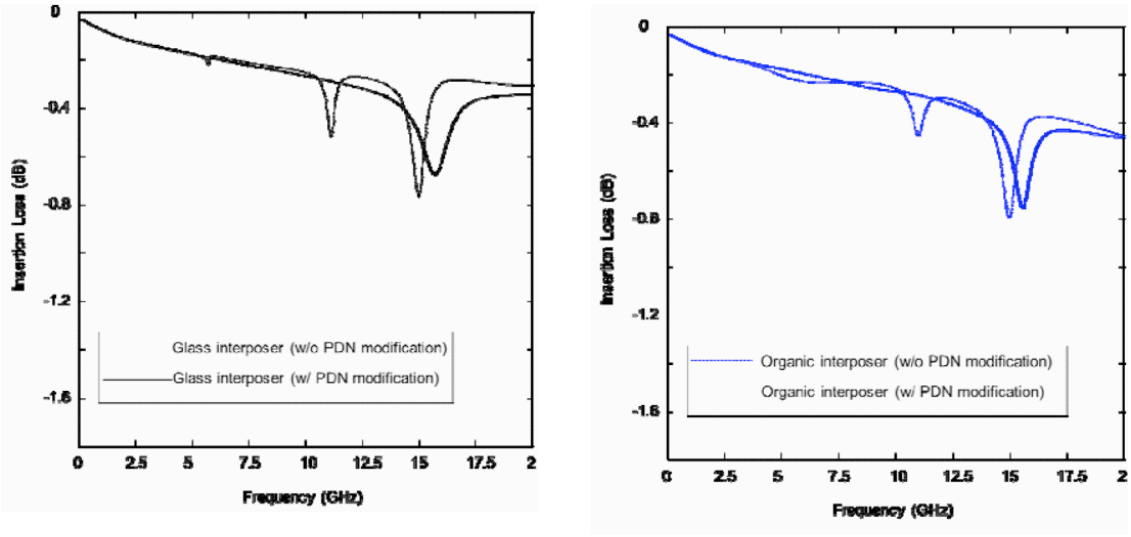


Figure 30. PDN induced insertion loss for organic and glass interposers [46].

External I/O performance on wafer-based silicon interposers was limited by wafer resistivity (doping), silicon bias, TSV oxide thickness, and ILD thickness [6, 19]. These metrics increased insertion loss if not considered for high speed design, and limited line length of external I/O to maintain performance budgets. This presented a design tradeoff in silicon interposer size—HPC system requirements required larger than reticle interposers to increase integration and system throughput, while smaller silicon interposers were best for external I/O performance [38].

The review of 2.5-D interposer technologies in 0 showed that organic and glass interposers are being considered to increase 2.5-D interposer size at lower cost compared to wafer-based silicon. The design of external I/O using glass and organic materials considered the effect of PDN resonance on insertion loss [46]. Increased loss was due to

the return path discontinuity at TPV and the tendency of the return path to flow through the substrate. The low electrical loss exhibited by glass and organic cores led to PDN resonance according to the cavity size created by the reference planes. This resulted in increased insertion loss at resonant frequencies as shown in Figure 30.

2.3 Summary

The electrical design of high density, wide I/O and high speed, external I/O was reviewed for 2.5-D silicon interposer. The design of wide I/O channels required decreased resistance, capacitance and channel length to meet interconnect bandwidth requirements that were dictated by the minimum signal rise time. Wide I/O interconnect delay, or RC time constant τ, was limited by BEOL design rules which set a critical path length on the order of 5 mm for wide I/O at 2 Gbps and rise time Δt = 0.2 UI. Electrical co-design of silicon interposer, substrate, and board were required to maintain external I/O performance budgets. External I/O performance was limited by TSV capacitive loading, TSV crosstalk, and RDL coupling loss to the silicon substrate. High wafer resistivity, increased TSV oxide thickness, and thick ILD thickness improved TSV performance. Stack-ups that increased shielding between RDL and silicon were used to improve line attenuation to approximately -0.5 dB/mm.

The 2.5-D glass interposer package presented in this thesis used high density RDL at line pitch and width approaching BEOL design rule with thick metallization by SAP to improve wide I/O performance. Smooth surface finish and low total thickness variation of glass enabled interconnect line width scaling, while high modulus and dimensional stability of glass allowed for microvia scaling. Furthermore, RDL on glass is used to

improve external I/O performance. Low dielectric constant and loss tangent compared to silicon decreased insertion loss at high frequencies.

CHAPTER 3. MODELING, DESIGN, FABRICATION AND CHARACTERIZATION OF RDL FOR WIDE I/O

This chapter describes the research on addressing the fundamental electrical design challenges associated with wide I/O interconnects described in Chapter 1, leading to the demonstration of low latency interconnects on glass interposers, as shown in Figure 31. Although wide I/O interconnects implemented in multilayer RDL have been analyzed for silicon interposers with BEOL processing, this research represents the first comprehensive analysis of higher aspect ratio, and hence lower resistance interconnects for wide I/O implemented in multilayer RDL on panel glass interposers.

A distinct advantage of glass over organic laminates used for traditional packages is its exceptional dimensional stability during panel processing. Compared to wafer-based silicon interposer RDL, panel processes were used to increase conductor cross section to

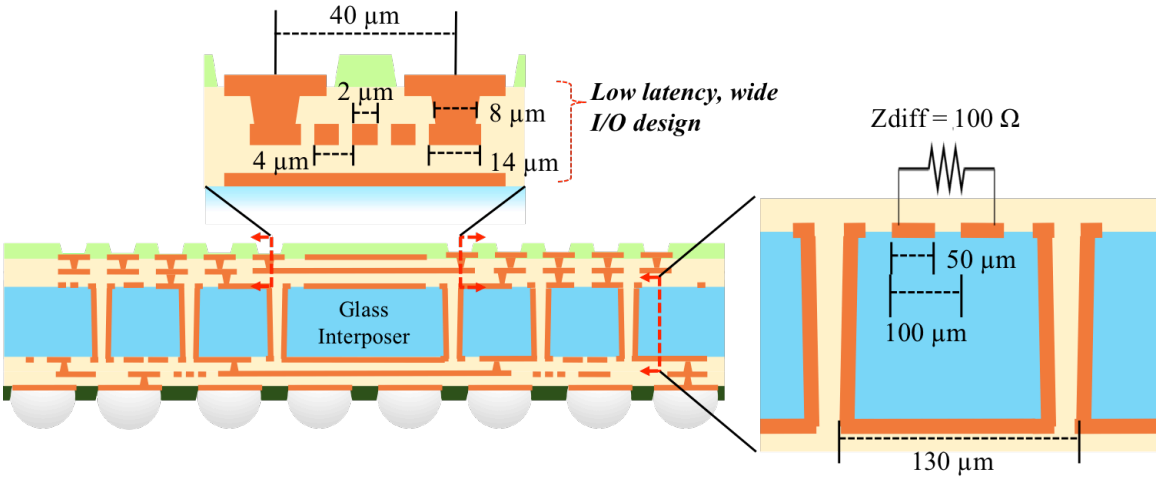


Figure 31. 2.5-D glass interposer with high density wide I/O.

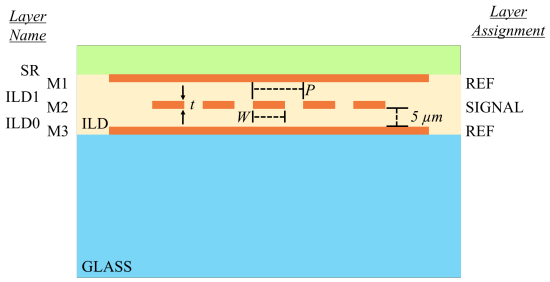
improve line latency and performance for high density die-to-die interconnects. The research goal in this chapter is to develop a design guideline for wide I/O on glass interposers using high copper height to line width ratio (*AR*). The main electrical design challenge to address is the increased capacitance and inductance with increasing line density.

The modeling, design, fabrication, and characterization of high density RDL with high *AR* to address these design challenges is described below. The modeling and simulation of wide I/O is organized into three sub-sections. First interconnect resistance, capacitance, and inductance were compared for different wide I/O signal layer assignments. Second, a wide I/O interconnect model was developed based on these parametric analyses to simulate interconnect delay as function of *AR*. Finally, interconnect delay for a wide I/O signal bus was simulated to determine the effect of crosstalk on signal latency. Interconnect latency and its dependence on *AR* is validated using fine pitch RDL high frequency test structures compatible with glass panel fabrication processes.

3.1 Low Latency Interconnect Modeling and Simulation

The modeling and simulation of die-to-die interconnects assumed an RDL stack with three-metal layers on the top side of the glass core as shown in Figure 32 where TPVs were not included in the die-to-die signal path. Two variations in signal layer assignment were analyzed including a ground-signal-ground (G-S-G) structure suitable for a stripline RDL geometry on metal layer 2 (M2-SL) and a signal-ground-signal (S-G-

Ground-Signal-Ground (G-S-G) Stack-up



Signal-Ground-Signal (S-G-S) Stack-up

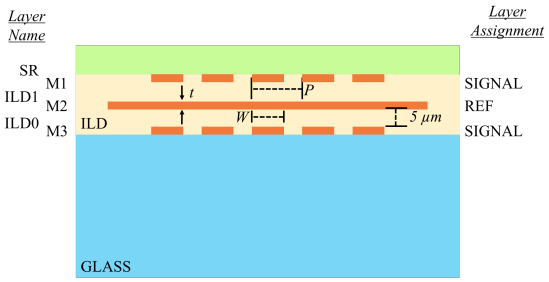


Figure 32. Wide I/O stack-up and signal layer assignments.

S) structure suitable for microstrip RDL geometries on metal layer 1 (M1-MSL) or metal layer 3 (M3-MSL).

The material properties used for the wide I/O modeling and design are summarized in Table 3. The glass material properties were provided by Asahi Glass Company (AGC) for the EN-A1^{TM} glass. Three thin film polymer dielectrics with different electrical properties were included in modeling and simulation with material properties in line with commercially available thin film polymers. To reduce the design space, an interlayer dielectric thickness of 5 μm was assumed for all dielectrics, and the material properties were assumed to be independent of dielectric film thickness. Electrical properties for a high resolution solder resist material comparable to properties provided by Hitachi Chemical were assumed for the passivation layer.

The thin film polymer types chosen for the interlayer dielectric material provide a suitable design space to study high density interconnect latency and performance. Compared to silicon dioxide (ε_r = 3.4 and $tan\delta$ = 0.01), ILD-A has low permittivity and a

Table 3. Glass, thin film polymer dielectrics, and solder resist material properties.

Material	ε_r (frequency)	$tan\delta$ (frequency)
Glass	5.3 (2.4 GHz)	0.004 (2.4 GHz)
ILD-A	3.2 (5.8 GHz)	0.017 (5.8 GHz)
ILD-B	3.0 (10 GHz)	0.005 (10 GHz)
ILD-C	2.5 (10 GHz)	0.002 (10 GHz)
Solder Resist	2.1 (10 GHz)	0.008 (10 GHz)

comparable loss factor; ILD-B has lower permittivity and low loss factor, while ILD-C has the lowest permittivity and lowest loss factor. The same solder resist material was used in all stack-ups.

3.1.1 Interconnect Resistance, Inductance, and Capacitance

A 2D-EM simulation tool available from ANSYS™ was used to extract resistance (r), inductance (l), and capacitance (c) per unit length transmission line parameters for an isolated wide I/O interconnect at 1 GHz. Line characteristics were extracted for three RDL geometries including M1-MSL, M2-SL, and M3-MSL using the stack-ups and material properties shown in Figure 32 and Table 3 respectively. Nine variations were included for each line geometry where copper thickness was varied from t = 1 μm, 5 μm,

and 10 μm and line width W was varied from W = 1 μm, 2 μm, and 3 μm for each copper thickness. The results of this parametric study are shown in Table 4.

Transmission line parameters summarized in Table 4 show that line resistance per unit length r at 1 GHz was independent of dielectric material properties and RDL stack-up. In general, r was inversely proportional to trace area, and skin effect was significant with increased trace thickness t = 5 μm and t = 10 μm. A skin depth δ_s = 2 μm at 1 GHz in bulk annealed copper reduced r by up to 40% compared to DC resistance. Inductance per unit length l was independent of dielectric material properties given that μ_r = 1.0 for ILD materials considered. In general, l decreased linearly with line width and was inversely proportional to copper thickness. Also, a stripline transmission line structure reduced l compared to microstrip line structures since the return path is split between top- and bottom-side ground layers. Capacitance per unit length c was dependent on dielectric material properties, RDL stack-up, and line geometry. Line capacitance decreased according to ILD permittivity with ILD-C exhibiting the lowest c with a fixed RDL stack-up and line geometry. A stripline RDL stack-up increased capacitive loading compared to microstrip line stack-ups studied. Microstrip line stack-ups reduced c but effective permittivity must be considered when determining interconnect capacitance. The effective permittivity was higher for lines routed on a metal layer 3 microstrip line compared to metal layer 1 microstrip lines which increased capacitive loading.

Signal behavior was determined before modeling interconnect delay. Two conditions were considered to determine if the interconnect exhibited transmission line (inductive) behavior or distributed RC (capacitive) behavior [47]:

Table 4. Transmission line parameters for RDL geometries at 1 GHz.

t	*W*	M1-MSL				M2-SL				M3-MSL			
µm	µm	r Ω/mm	l pH/mm	c fF/mm	Z0 Ω	r Ω/mm	l pH/mm	c fF/mm	Z0 Ω	r Ω/mm	l pH/mm	c fF/mm	Z0 Ω
						ILD-A							
1	1	17.6	671	48	244	17.6	583	72	199	17.6	671	72	199
	2	9.0	591	55	167	9.0	502	85	133	9.0	591	83	136
	3	6.1	534	62	133	6.1	445	97	104	6.1	533	93	109
5	1	3.6	511	71	103	3.6	417	104	82	3.6	511	93	90
	2	1.9	480	78	85	1.9	387	116	64	1.9	480	102	74
	3	1.3	453	84	76	1.3	360	128	56	1.3	453	110	67
10	1	1.9	438	87	77	1.9	342	128	59	1.9	438	107	70
	2	1.0	418	94	69	1.0	323	140	50	1.0	417	115	62
	3	0.8	399	100	64	0.7	305	152	46	0.8	399	123	58
						ILD-B							
1	1	17.6	671	45	251	17.6	583	67	205	17.6	671	69	203
	2	9.0	591	52	171	9.0	502	80	137	9.0	591	80	139
	3	6.1	534	59	137	6.1	445	91	108	6.1	533	89	111
5	1	3.6	511	67	106	3.6	417	97	85	3.6	511	88	93
	2	1.9	480	73	87	1.9	387	109	66	1.9	480	97	76
	3	1.3	453	80	79	1.3	360	120	58	1.3	453	105	68
10	1	1.9	438	82	80	1.9	342	120	61	1.9	438	101	72
	2	1.0	418	88	71	1.0	323	132	52	1.0	418	109	64
	3	0.8	399	94	66	0.7	305	143	47	0.8	399	117	59
						ILD-C							
1	1	17.6	671	39	272	17.6	583	56	225	17.6	671	62	214
	2	9.0	591	45	185	9.0	502	67	150	9.0	591	72	146
	3	6.1	534	50	148	6.1	445	76	118	6.1	534	80	117
5	1	3.6	511	57	116	3.6	417	81	93	3.6	511	78	99
	2	1.9	480	62	95	1.9	387	91	73	1.9	480	85	81
	3	1.3	453	67	85	1.3	360	100	64	1.3	453	92	73
10	1	1.9	438	69	87	1.9	342	100	67	1.9	438	88	77
	2	1.0	418	75	77	1.0	323	110	57	1.0	418	95	68
	3	0.8	399	80	72	0.7	305	119	52	0.8	399	101	64

1. 2.5 $t_f > t_r$

2. R < $5Z_0$

For condition (1), t_f is the time of flight for the transmission line and t_r is the signal rise time. Time of flight, determined using line parameters in Table 4, was used to calculate the critical line length for inductive signal behavior L_1 such that

$$L_1 > v_p \frac{t_r}{2.5} = \frac{t_r}{2.5\sqrt{lc}} \quad (11).$$

The critical line length for capacitive signal behavior L_2 was also determined using line parameters in Table 4 where

$$L_2 < \frac{5}{r}\sqrt{\frac{l}{c}} \quad (12).$$

Table 5 summarizes these critical line lengths based on the RDL geometries simulated and was used to determine interconnect model parameters for delay simulations. A rise time t_r = 100 ps consistent with 2 Gbps wide I/O signaling was used for these calculations.

The average inductive critical line length was L_{1_avg} = 6.5 mm based on signal condition (1). Transmission line behavior, however, was dominant compared to capacitive signal behavior due to low line resistance compared to the line characteristic impedance at 1 GHz based on signal condition (2). Therefore, to determine interconnect

Table 5. Critical line lengths for inductive (L_1) and capacitive (L_2) signal behavior.

t	W	M1-MSL			M2-SL			M3-MSL		
µm	µm	Z_0 Ω	L_1 mm	L_2 mm	Z_0 Ω	L_1 mm	L_2 mm	Z_0 Ω	L_1 mm	L_2 mm
					ILD-A					
1	1	244	7.05	33.59	199	6.17	25.56	199	5.75	27.43
	2	167	7.02	57.59	133	6.12	42.69	136	5.71	46.88
	3	133	6.95	76.07	104	6.09	55.52	109	5.68	62.05
5	1	103	6.64	117.83	82	6.07	87.95	90	5.80	102.95
	2	85	6.54	206.44	64	5.97	152.00	74	5.72	180.52
	3	76	6.48	282.45	56	5.89	203.97	67	5.67	246.82
10	1	77	6.48	186.72	59	6.05	136.03	70	5.84	168.37
	2	69	6.38	333.42	50	5.95	240.16	62	5.78	301.08
	3	64	6.33	394.79	46	5.87	319.96	58	5.71	355.97
					ILD-B					
1	1	251	7.28	34.69	205	6.40	26.50	203	5.88	28.02
	2	171	7.22	59.23	137	6.31	44.01	139	5.82	47.75
	3	137	7.13	77.98	108	6.29	57.32	111	5.81	63.43
5	1	106	6.84	121.29	85	6.29	91.06	93	5.96	105.84
	2	87	6.76	213.39	66	6.16	156.80	76	5.86	185.12
	3	79	6.64	289.42	58	6.09	210.66	68	5.80	252.63
10	1	80	6.67	192.33	61	6.24	140.49	72	6.01	173.30
	2	71	6.60	344.60	52	6.13	247.33	64	5.93	309.63
	3	66	6.53	407.20	47	6.06	329.88	59	5.85	364.98
					ILD-C					
1	1	272	7.82	37.26	225	7.00	28.99	214	6.20	29.55
	2	185	7.76	63.67	150	6.90	48.09	146	6.13	50.33
	3	148	7.74	84.71	118	6.88	62.72	117	6.12	66.97
5	1	116	7.41	131.50	93	6.88	99.65	99	6.34	112.42
	2	95	7.33	231.55	73	6.74	171.61	81	6.26	197.76
	3	85	7.26	316.26	64	6.67	230.77	73	6.20	269.89
10	1	87	7.28	209.67	67	6.84	153.90	77	6.44	185.66
	2	77	7.14	373.27	57	6.71	270.94	68	6.35	331.66
	3	72	7.08	441.39	52	6.64	361.62	64	6.30	392.83

delay, a low loss transmission line model is preferred to a distributed or lumped element interconnect model to include inductive effects on interconnect delay.

3.1.2 Interconnect Delay Simulation

Interconnect delay was simulated in Keysight Advanced Design System using the test bench shown in Figure 33. The voltage source used a step function with voltage and rise time values consistent with those used for the design of a silicon interposer. The source impedance was considered when simulating interconnect delay, and a linear model for the source resistance R_s = 10 Ω was used. On-chip loads $C_{Tx} = C_{Rx}$ = 0.4 pF were also assumed. Analysis in 0 showed that the wide I/O interconnect behaved as a low loss

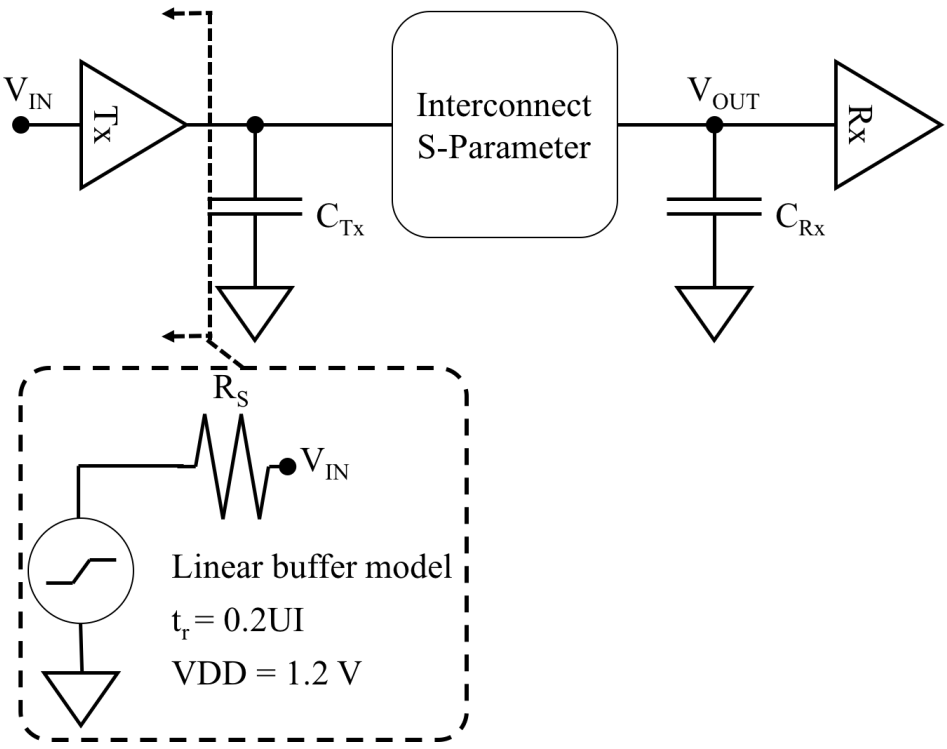


Figure 33. Interconnect delay test bench.

transmission line, and, therefore, the interconnect model used S-parameters simulated in ANSYS™ Electronic Desktop from 0.05 GHz to 20 GHz at a 0.05 GHz frequency step.

The design space for wide I/O interconnect RDL geometry summarized in Table 4 was down selected based on line pitch and width to meet line density requirements for wide I/O implemented using BEOL design rules on silicon interposers. Therefore, interconnect delay was simulated for line width $W = 2$ µm at copper thickness $t = 1$ µm, 5 µm, and 10 µm. The results of this simulation using a G-S-G topside glass interposer stack-up and ILD-A are shown in Figure 34 for a line length of $L = 5$ mm and compared to the RC delay of a silicon interposer with $r_{Si} = 6.5$ Ω/mm and $c_{Si} = 250$ fF/mm [31].

The simulated step response and its dependence on RDL copper trace thickness in

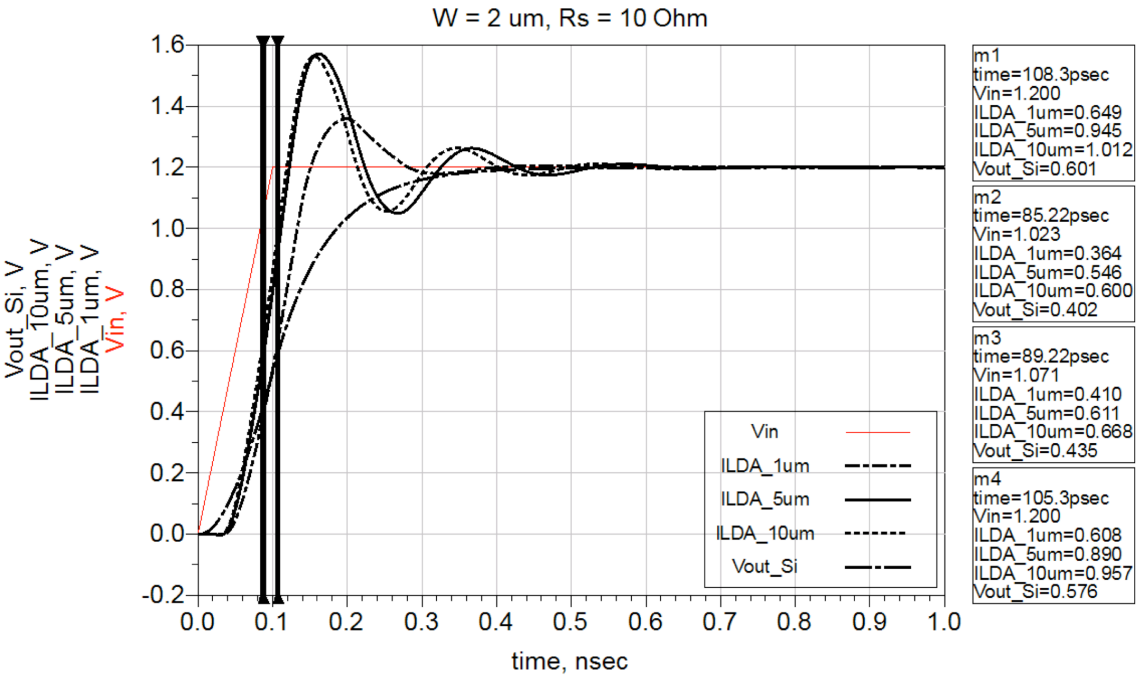


Figure 34. The effect of copper thickness on M2-SL interconnect delay.

Figure 34 clearly shows the inductive behavior of the wide I/O interconnect. At decreased copper thickness, however, line resistance increased and the transmission line behavior was less dominant and approached capacitive behavior exhibited by the highly resistive BEOL silicon interposer interconnect.

Simulated interconnect delay T_d was calculated at $V_{OUT} = 0.5V_{IN}$. These delay times are highlighted in Figure 34 for each RDL geometry. In general, T_d decreased with increased copper thickness. The simulated interconnect delay for t = 5 µm and t = 10 µm at W = 2 µm was T_d = 0.078 and T_d = 0.070 respectively, and, for t = 1 µm, the interconnect delay converged to the delay of a BEOL interconnect T_d = 0.12 UI. Therefore, increasing trace cross section by 5x and 10x decreased interconnect delay

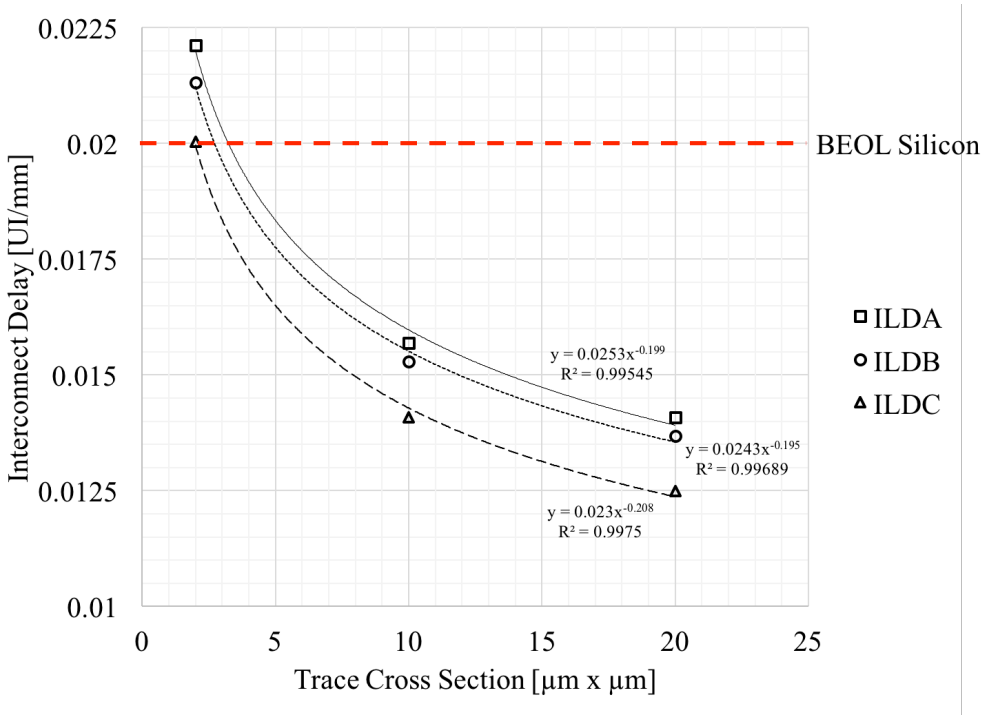


Figure 35. Interconnect delay as a function of trace cross section.

anywhere from 35% to 40% relative to BEOL wide I/O interconnect geometries. Interconnect delay per unit length t_d is shown as a function of trace cross section A in Figure 35 for a G-S-G interposer stack-up using thin film polymer dielectrics listed in Table 3. These interconnect delay simulation results showed a strong correlation between t_d and A where t_d was shown to vary indirectly to $\sqrt[5]{A}$ for each of dielectric materials studied. Furthermore, a cross section greater than 5 μm^2 was required to reduce delay below wafer-based silicon interposer wide I/O.

It was shown that interconnect capacitance and inductance per unit length depended on layer assignment. Specifically, a G-S-G stack-up decreased l compared to a S-G-S stack-up, but increased capacitive loading. A S-G-S stack-up reduced c but effective

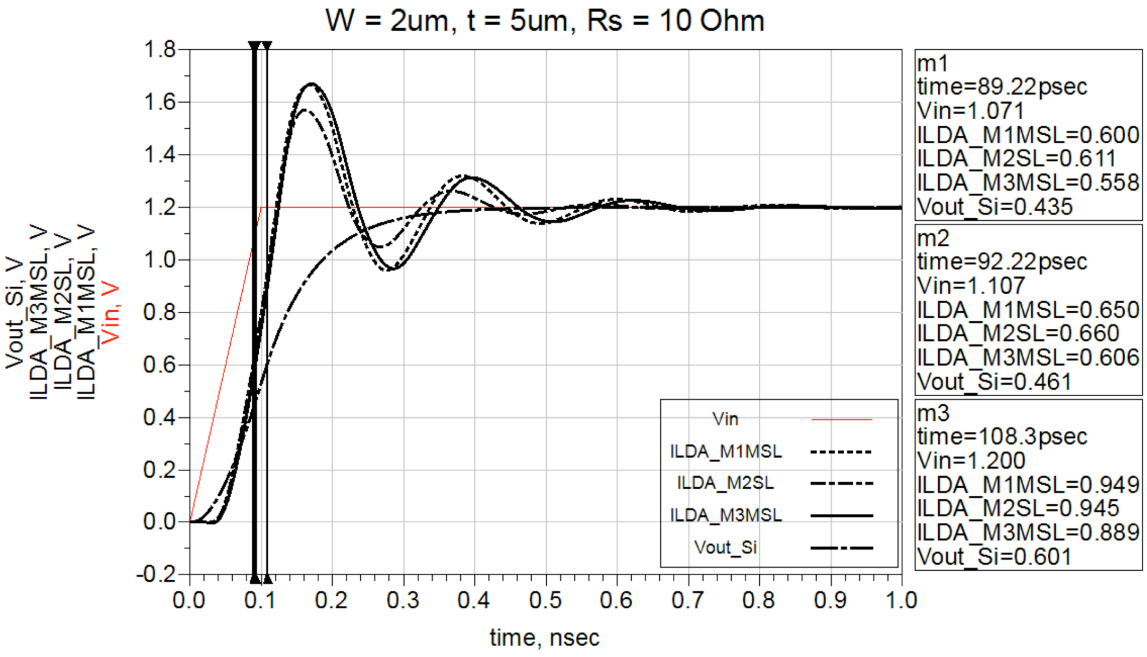


Figure 36. Stack-up dependent interconnect delay.

permittivity depended on signal layer assignment. Figure 36 compares the interconnect delay for each type of RDL stack-up considered at W = 2 um and t = 5 um. Each RDL geometry exhibited a lower delay relative to a BEOL silicon interconnect in accordance with analysis shown in Figure 35. Interconnect delay for the M1-MSL and M2-SL were comparable t_d = 0.015 UI/mm, but the lower inductance of the M2-SL reduced ringing at V_{OUT}. Increased line capacitance due to higher effective permittivity of a M3-MSL channel, however, increased line delay by 4 ps compared to the M1-MSL.

3.1.3 Wide I/O Signal Bus Delay Simulation

Interconnect resistance, inductance, capacitance, and delay per unit length were simulated for various line widths and copper thicknesses in 0 and 3.1.2. It was shown that increased trace cross section A reduced interconnect delay, but the effect of crosstalk on interconnect delay must be considered with increasing copper thickness. Crosstalk analysis required a wide I/O signal bus model. Model generation considered the effect of microvia padstack along with line pitch and width on line density.

Microvia padstack consisted of the via landing pad, via capture pad, and via diameters. A general die escape routing structure is shown for chip level interconnect bump pitch D in Figure 37. The following analysis assumed D = 40 μm in order to align with research objectives described in Table 2.

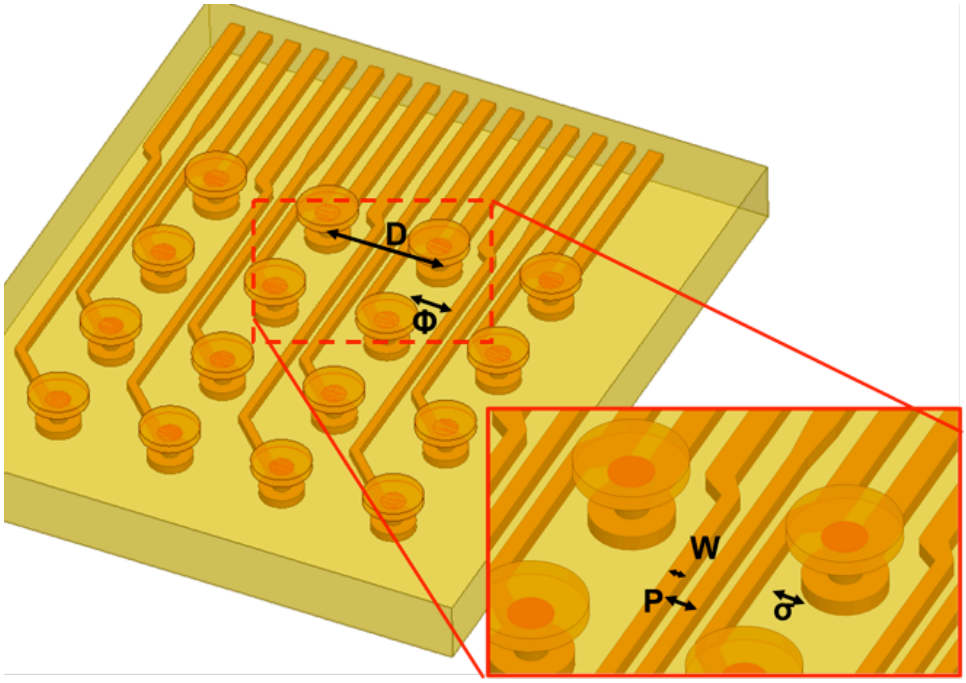


Figure 37. Die escape SAP RDL density parameters.

Lithography alignment, substrate dimensional stability, and via drill alignment were the main contributing factors to the size of a microvia capture pad. As mentioned previously, the dimensional stability of glass was an advantage compared to traditional organic package substrates to aggressively scale microvia padstack dimensions and effectively increase wide I/O line density. The dependence on the number of lines n routed between two microvia capture pads of diameter Φ at pitch D is defined by Equation 3 where σ is pad to line space, P is line pitch, W is line width determined by RDL design rules, and D is determined by the microvia process as depicted in Figure 37.

$$n \leq \frac{(D+P)\text{-}(2\sigma + \Phi + \mathrm{W})}{P} \tag{13}$$

Given the number of lines escaped and the in-line escape geometry shown Figure 37, the line density δ (lines/mm) for a single routing layer is defined by Equation 4 where pad pitch D is in microns.

$$\delta = \frac{1000\ (n+1)}{D} \tag{14}$$

The dependence of routing density on capture pad size Φ = 5 – 25 µm is shown in Figure 38 for D = 40 µm at various line pitch and width. Microvia capture pad diameters below 10 µm were suitable to escape up to five interior rows to achieve δ = 150

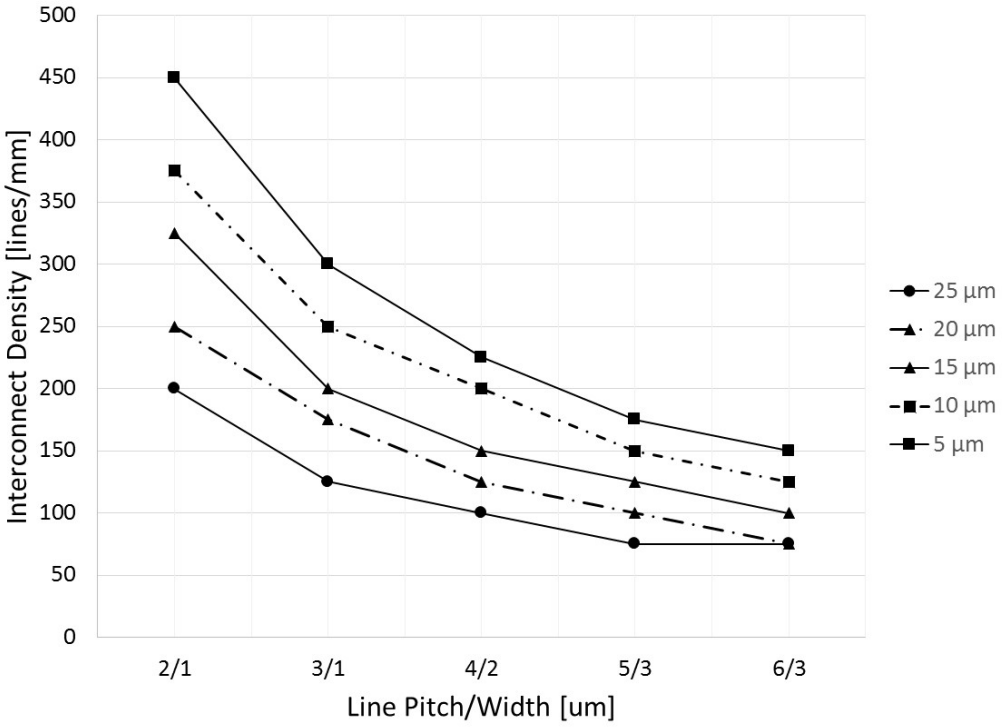


Figure 38. Effect of RDL geometry on interconnect density.

lines/mm·layer at 6 µm line pitch. This line density was comparable to wafer-based silicon interposer line density, and showed that scaling microvia padstack was critical to increase wide I/O interconnect density.

Wide I/O bus simulations assumed microvia capture pads below 10 µm, and, as a result, line pitch and width fan out after die escape routing was not allowed. In other words, line cross section was maintained across the length of the die-to-die interconnect. This was reflected in the model used for 3D-EM simulation of the wide I/O die-to-die interface as shown in Figure 39.

Line pitch and width and copper height were chosen to achieve Z_0 = 50 Ω with a 5 µm interlayer dielectric thickness. Based on simulation results in Table 4, a G-S-G stack-

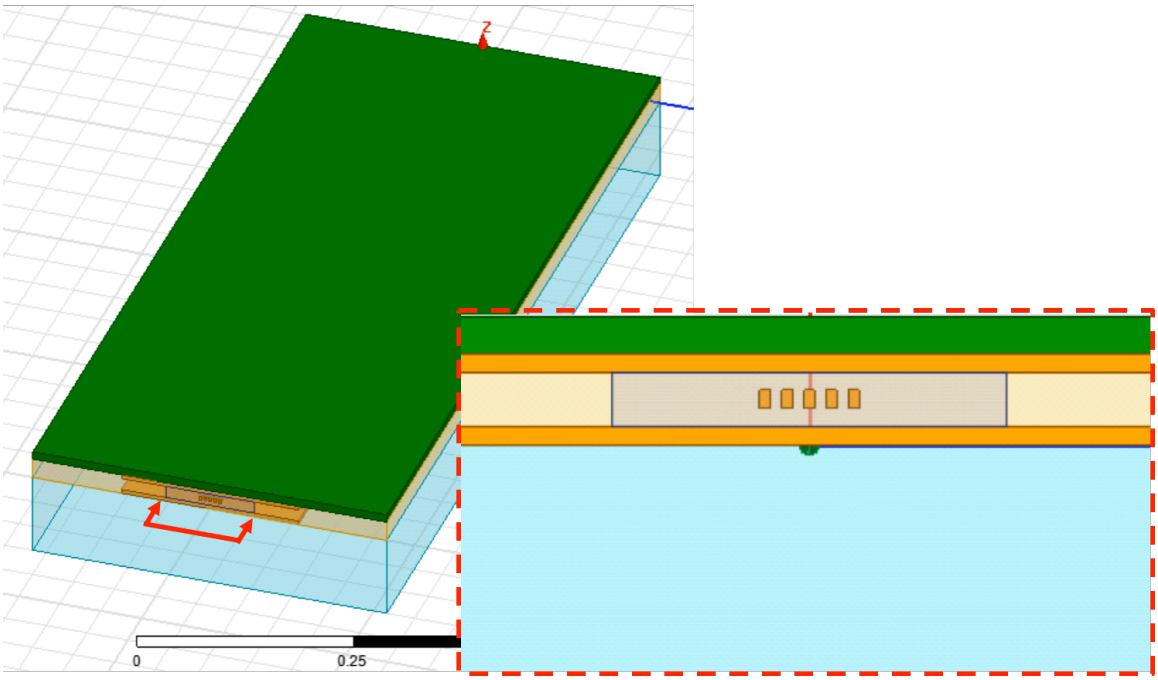


Figure 39. Wide I/O bus interconnect model.

up was used with two line variations:

1. W = 3 µm (P = 6 µm) and t = 5 µm.
2. W = 2 µm (P = 4 µm) and t = 10 µm.

Line performance was simulated from 0.05 GHz up to 20 GHz at a 0.05 GHz frequency step and S-parameter model files were generated using ANSYS™ Electronic Desktop. Interconnect delay was simulated using a test bench similar to Figure 33. Interconnect delay was calculated for the center line shown in the wide I/O bus interconnect model for a low to high transition from 0 V to 1.2 V at t_r = 100 ps. Surrounding traces, or aggressor lines were excited with a step voltage source out of phase with that of the channel of interest, or victim line. Aggressor lines were driven with

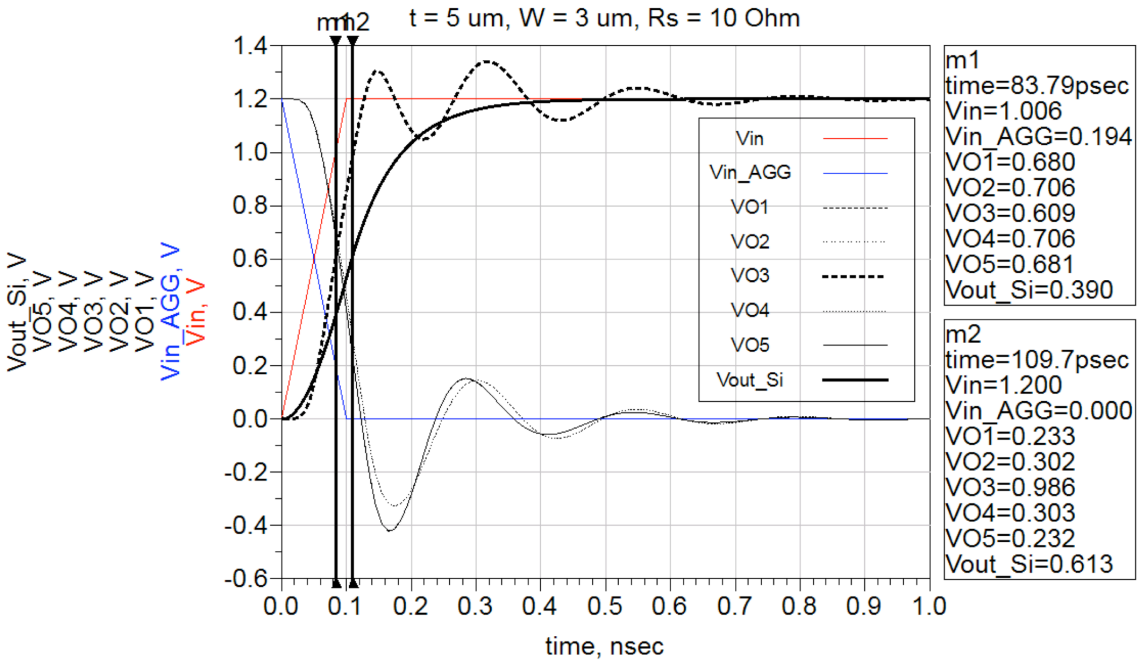


Figure 40. Wide I/O bus interconnect delay for design variation (1).

a high to low transition from 1.2 V to 0 V at a fall time t_f = 100 ps. This design choice was used to simulate the worst case switching scenario for a wide I/O bus [31].

The simulated step response for design variation (1) and (2) are shown in Figure 40 and Figure 41. The simulated interconnect delay for design variation (1) and (2) was t_d = 0.013 UI/mm and t_d = 0.017 UI/mm respectively. Interconnect delay followed the analysis for an isolated wide I/O channel discussed in 3.1.2—inductive signal behavior was observed and delay was less than the RC delay exhibited by high resistance BEOL interconnects. The effect of crosstalk on delay was significant. The interconnect delay was expected to decrease from design variations (1) to (2) based on the trend shown in Figure 35. Interconnect delay increased for design variation (2) relative to (1). This was

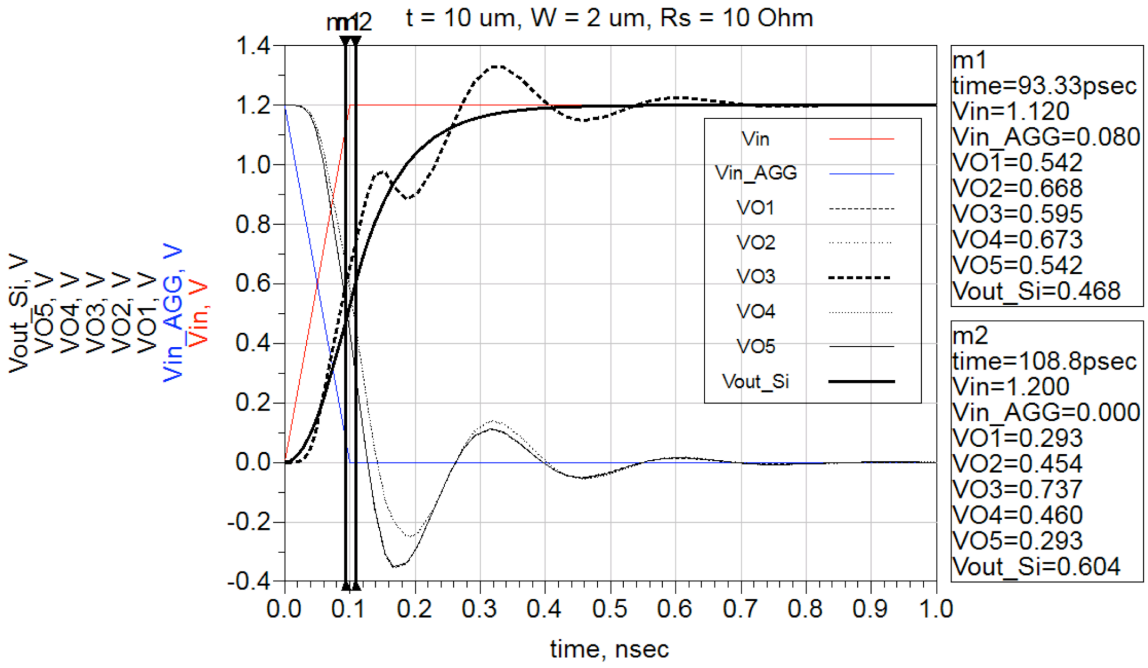


Figure 41. Wide I/O bus interconnect delay for design variation (2).

attributed to the additional capacitive and inductive coupling at t = 10 μm. Therefore, at a fixed dielectric thickness there existed a design tradeoff to reduce interconnect delay. Ground coupling was fixed by ILD thickness, and the victim line was more sensitive to crosstalk. To increase line density and copper thickness to improve wide I/O performance, it was recommended to decrease ILD thickness to increase ground coupling. In the case where ILD thickness was limited by manufacturability, guard traces were recommended to maintain line performance, but this decreased signal line density at the die edge.

3.2 Design and Characterization of Low Latency RDL

This section describes the design, fabrication, and characterization of high density RDL for wide I/O. The demonstration of these high density RDL was included in a 2.5-D glass interposer process test vehicle. The electrical design objective was to characterize fine line RDL geometries that were fabricated using double-sided and panel-scalable processes with interconnect lengths up to 25 mm.

3.2.1 Panel Layout and Design

The panel design for the wide I/O test vehicle is shown in Figure 42 and included three test coupon variations to address electrical and fabrication objectives. Test coupon A, shown in the middle Figure 42 detail, consisted of the fine pitch RDL high frequency test structures used to validate modeling and simulation results discussed in 3.1. The process test vehicle did not include microvia or TPV, and co-planar waveguides were used for high frequency tests.

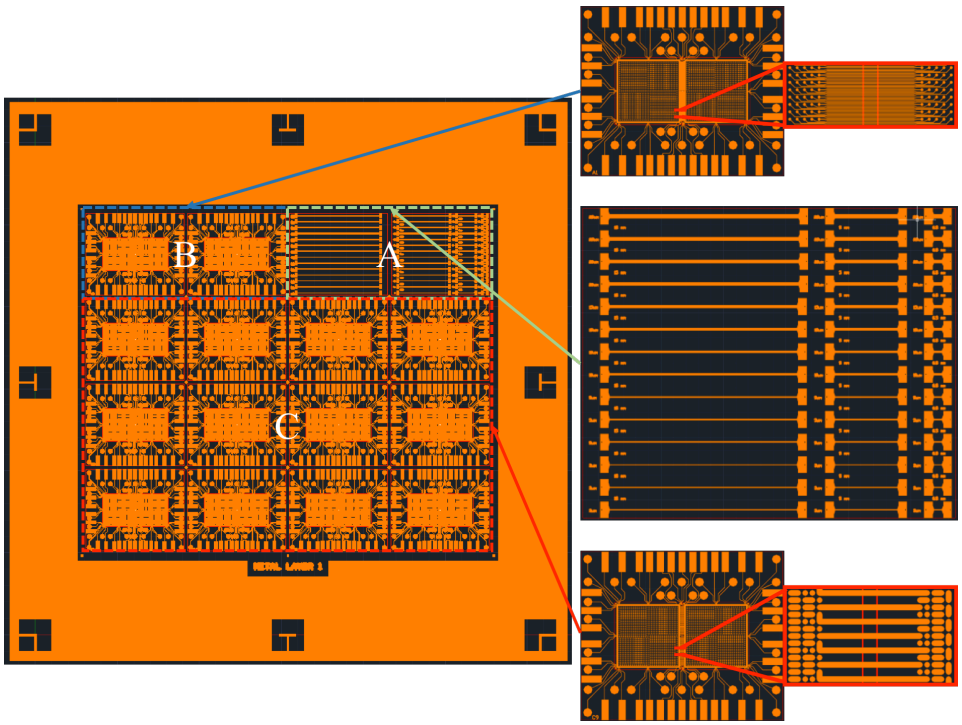
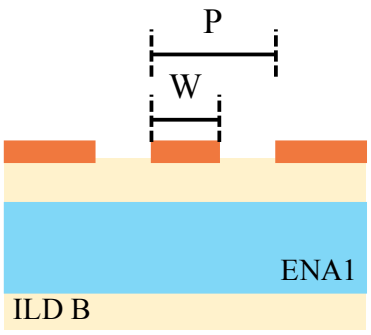


Figure 42. Wide I/O glass test vehicle panel layout.

The design rules for these high frequency test structures are summarized in Figure 43. Twenty-four CPW design variants were included with a minimum line pitch P = 7 µm. Six different signal widths from a minimum W = 3 µm up to W = 25 µm were included in test coupon A. Line spacing between the CPW signal line and ground trace was tuned to maintain a characteristic impedance Z_0 = 50 Ω (assuming ILD-B material properties shown in Table 3) for high frequency characterization using a vector network analyzer. For each signal width, four different signal lengths were included from a minimum L = 660 µm up to L = 25 mm.

Test coupon B, shown in the upper right Figure 42 detail, included a 2.5-D die-to-die escape routing structure on a 25mm x 30mm body size glass interposer with 879 die-



W [µm]	*P* [µm]
3	7
5	10
10	16
15	24
20	32
25	38

Figure 43. Fine pitch RDL high frequency test structure design rule summary.

to-die interconnections. A bump landing pad size of 20 µm on the top metal layer of the glass interposer enabled the routing of four interior signal rows in one layer with 3 µm wiring technology. Outside the die shadow, the traces fan out to 5 µm lines at 500 µm line length between the dies. Consequently, the largest line length at 6 µm RDL pitch was approximately 300 µm.

Test coupon C shown in the lower right Figure 42 detail, used a serpentine 2.5-D chip-level assembly test structure on a 25 mm x 30 mm glass interposer to evaluate fine pitch chip-level assembly processes. This assembly test structure had 87 die-to-die interconnections, and used a coarse 40 µm line and space for die-to-die routing.

3.2.2 Panel Process Flow and Fabrication

The six-metal layer wide I/O glass test vehicle was fabricated on 300 µm thick 150 mm x 150 mm glass panels provided by AGC without TPV. Panel processes discussed in [48] were used to fabricate the test structures described in 3.2.1. The double-sided panel process flow is summarized in Figure 44. Prior to SAP1, the glass surface

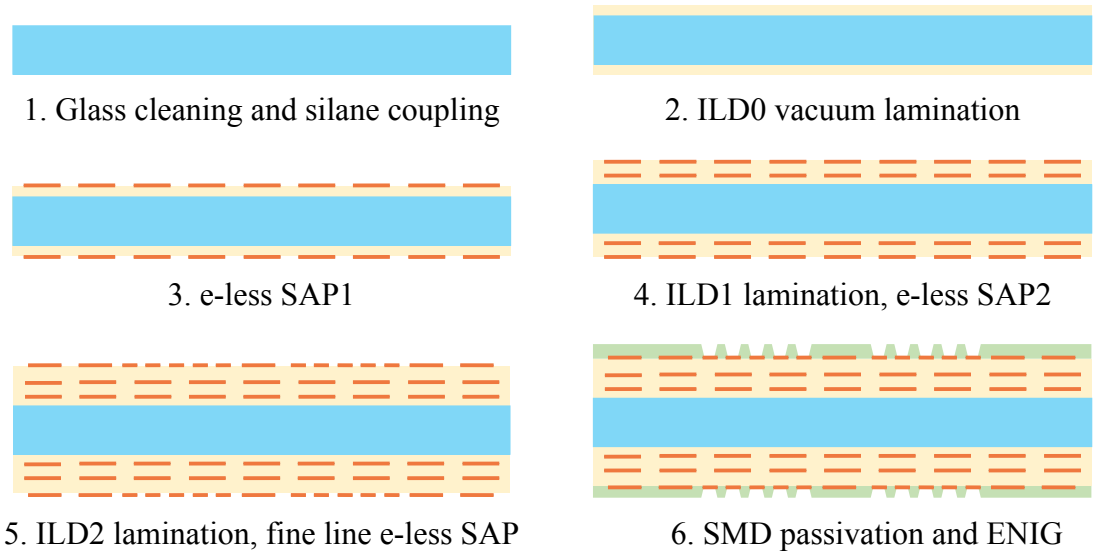


Figure 44. Six-metal layer glass test vehicle panel fabrication process flow.

was cleaned using successive methanol, acetone, and isopropanol rinses and a liquid silane layer was applied. The silane layer increased adhesion between the glass and dry thin film dielectric vacuum laminated on both sides of the panel before metallization. A total of three SAP RDL were used to fabricate a six-metal layer glass interposer. Internal SAP RDL consisted of a dummy mesh pattern at 55% copper coverage and were not interconnected with blind microvias. The process test vehicle used dummy mesh layers to emulate thermomechanical behavior of a 2.5-D glass interposer package and qualify 2.5-D chip-level assembly processes.

The top RDL layer included high density die-to-die interconnects and substrate assembly pad structures required for four-point probe test structures to verify die assembly. More importantly, the SAP with a palladium catalyzed electroless (e-less) copper seed layer was used to increase *AR* in accordance with electrical modeling results discussed in 3.1. The advanced e-less SAP to realize high aspect ratio RDL required three

enabling processes including Novalink®, projection lithography, and differential copper seed layer etch. Novalink® is an adhesion promoter provided by Atotech for dry film photoresist. This was required to reduce line pitch and width without resist collapse or delamination during the SAP. High resolution projection lithography provided by USHIO Inc. was used on panel at an optimized depth of focus and resist development time to avoid resist bridging and to resolve 6 µm pitch RDL geometries. Lastly, differential copper seed layer etch was used to realize fine line RDL structures without copper over etching and to improve line shape [49].

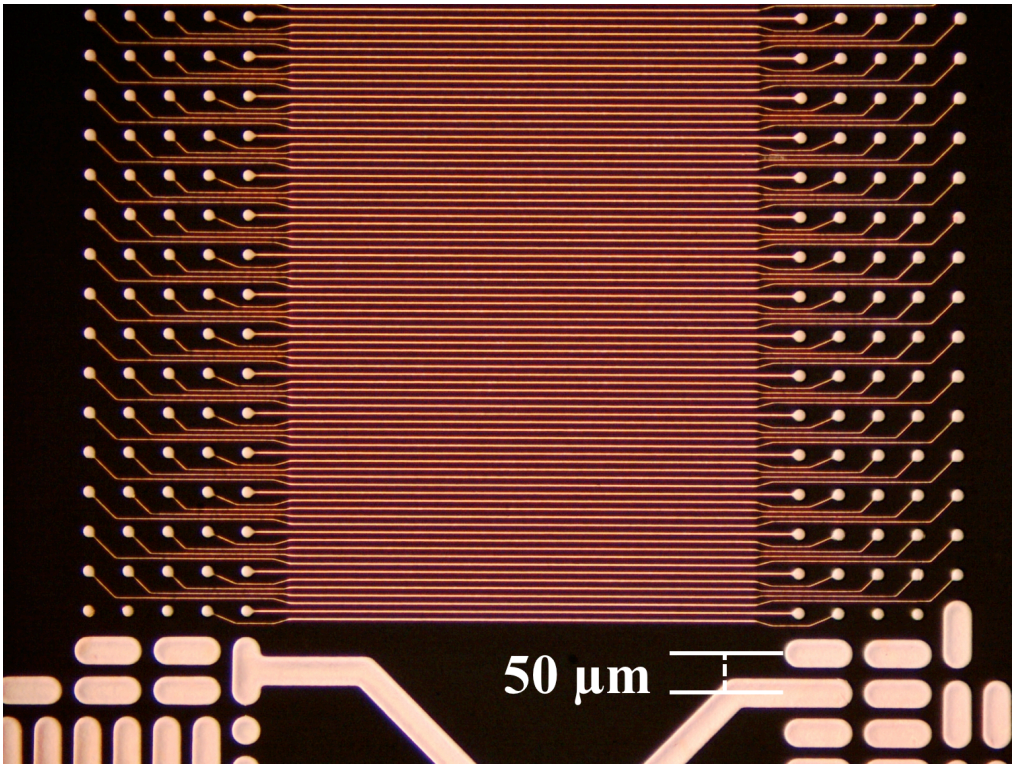


Figure 45. Fine line die-to-die routing at 50 µm bump pitch.

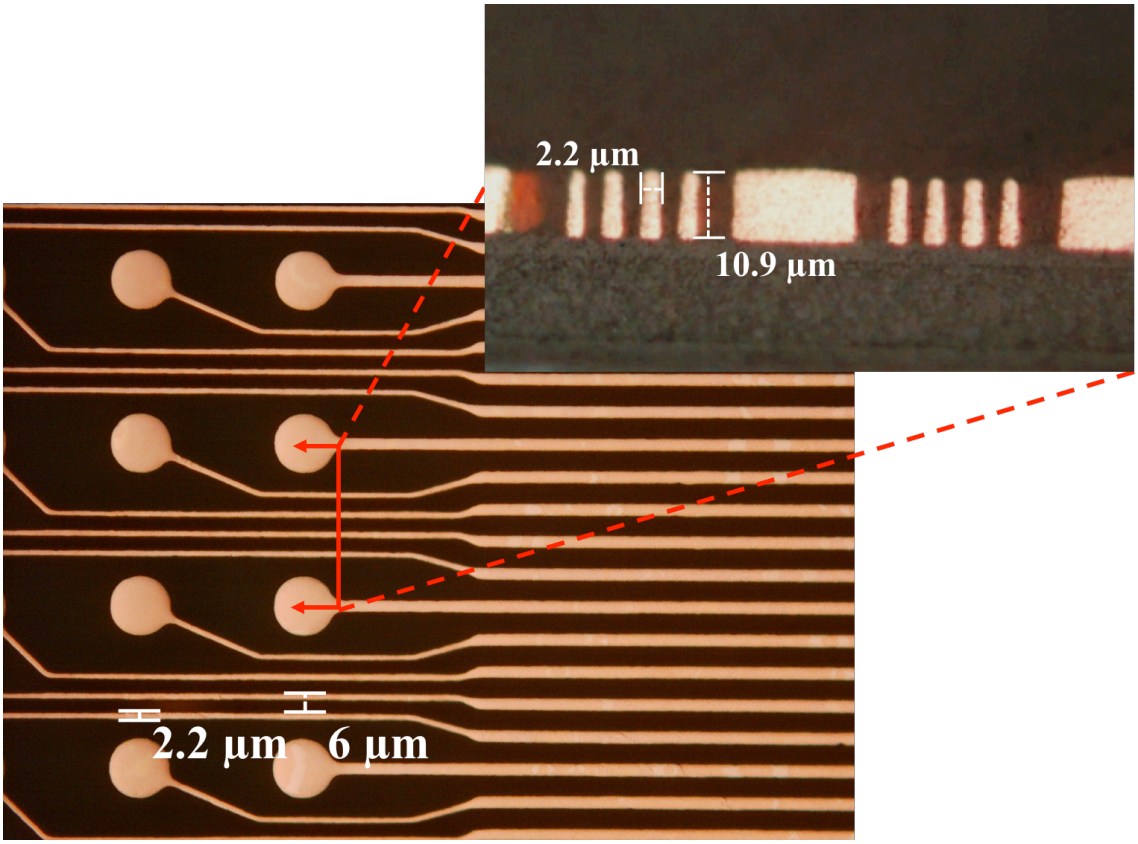
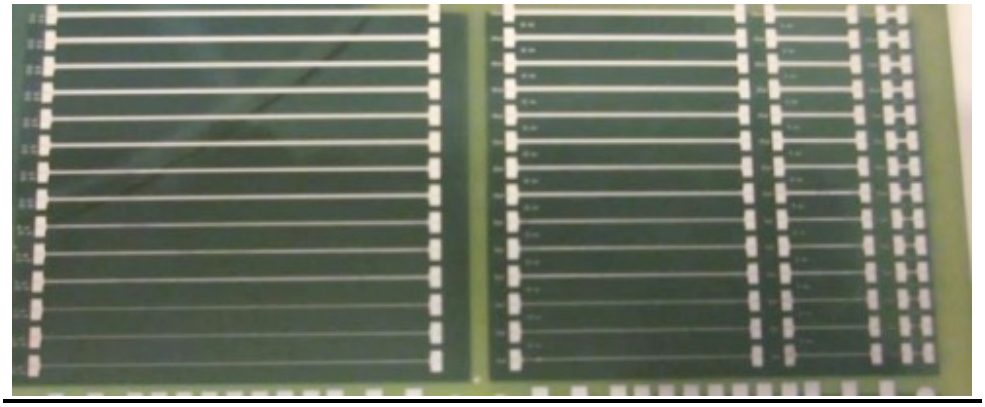


Figure 46. High aspect ratio 6 µm pitch RDL for low latency wide I/O.

Representative fabrication results of high aspect ratio, fine pitch RDL geometries using an e-less SAP are shown for test coupon B in Figure 45 and Figure 46. Optical inspection confirmed good yield of 6 µm pitch e-less SAP RDL to achieve 879 die-to-die interconnections without line delamination or bridging. Cross section was used to confirm an *AR* of approximately 5:1 for fine pitch RDL structures. Line narrowing was also observed despite localized differential copper seed layer etch. It was recommended to improve line width variation by mask compensation where compensation width must consider lithography limitations including resist resolution and adhesion.

3.2.3 Fine Line Characterization and Analysis

The following discusses the high frequency characterization and time domain analyses of fine pitch RDL for low latency wide I/O. Fabrication results for test coupon A containing the 24 high frequency test structure variations are shown in Figure 47. Parametric line lengths from L = 0.66 – 25 mm were used to qualify a maximum RDL



W	*L* = 25 mm	*L* = 15 mm	*L* = 5 mm	*L* = 0.66 mm
25 µm				
25 µm				
20 µm	X			
20 µm	X			
15 µm	X			
15 µm	X			
10 µm	X	X		
10 µm	X	X		
5 µm	X	X		
5 µm	X	X		
5 µm	X	X	X	
3 µm	X	X	X	
3 µm	X	X	X	
3 µm	X	X		

Figure 47. Test coupon A high frequency test structure yield matrix.

line length design rule. In general, the line yield increased with increasing line width where L = 25 mm at W = 25 um was achieved. The yield matrix in Figure 47 indicated low yield of W = 3 µm CPW structures beyond L = 5 mm which suggested the maximum die escape length at this line width using the RDL processes discussed in 3.2.2.

3.2.3.1 High Frequency Characterization

High frequency characterization was performed using a 2-port VNA with ACP50-GSG-500 probes available from Cascade MicroTech. A short-open-load-thru (SOLT)

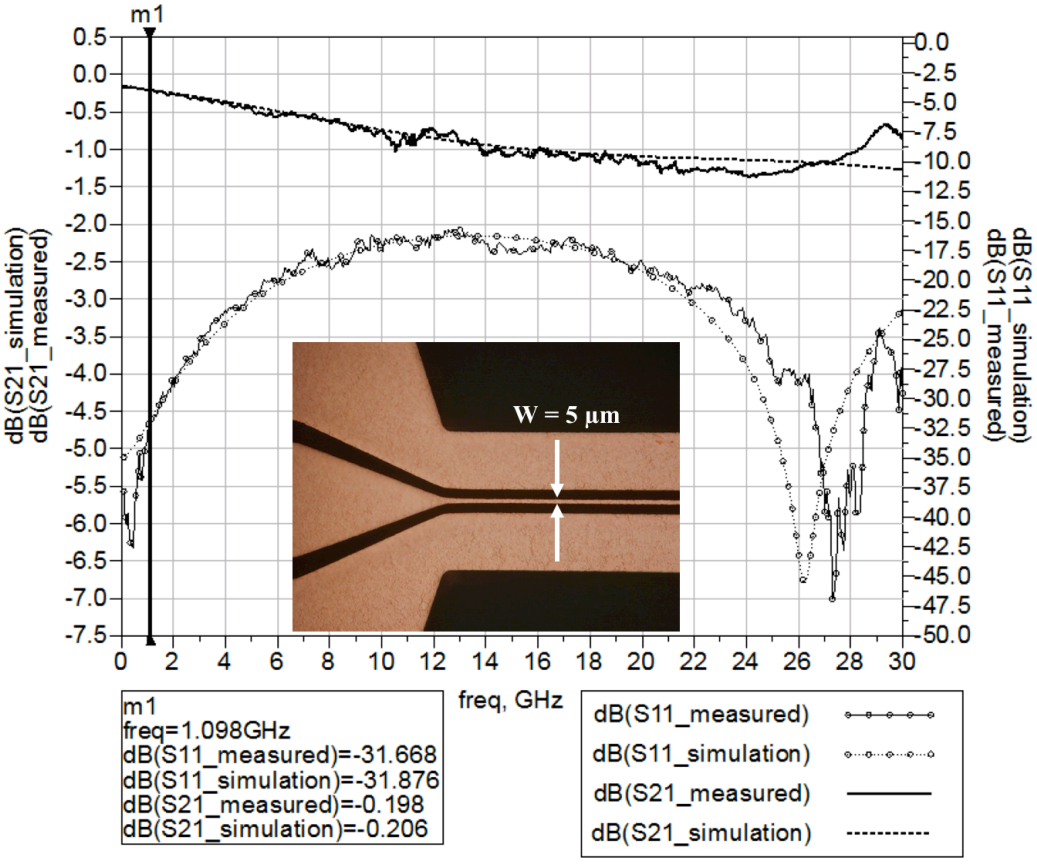


Figure 48. Characterization of W = 5 µm RDL at L = 5 mm.

calibration up to 30 GHz was performed prior to measurement using the Impedance Substrate Standard 106-628A available from Cascade MicroTech. The CPW structures were characterized from 100 MHz up to 30 GHz at 74.75 MHz intervals.

Measurement results are compared to simulation results performed using ANSYS™ Electronic Desktop for CPW structures with W = 5 µm and W = 3 µm in Figure 48 and Figure 49 respectively at L = 5 mm. Good model to hardware correlation was observed for both measurements. A shift in return loss was attributed to copper

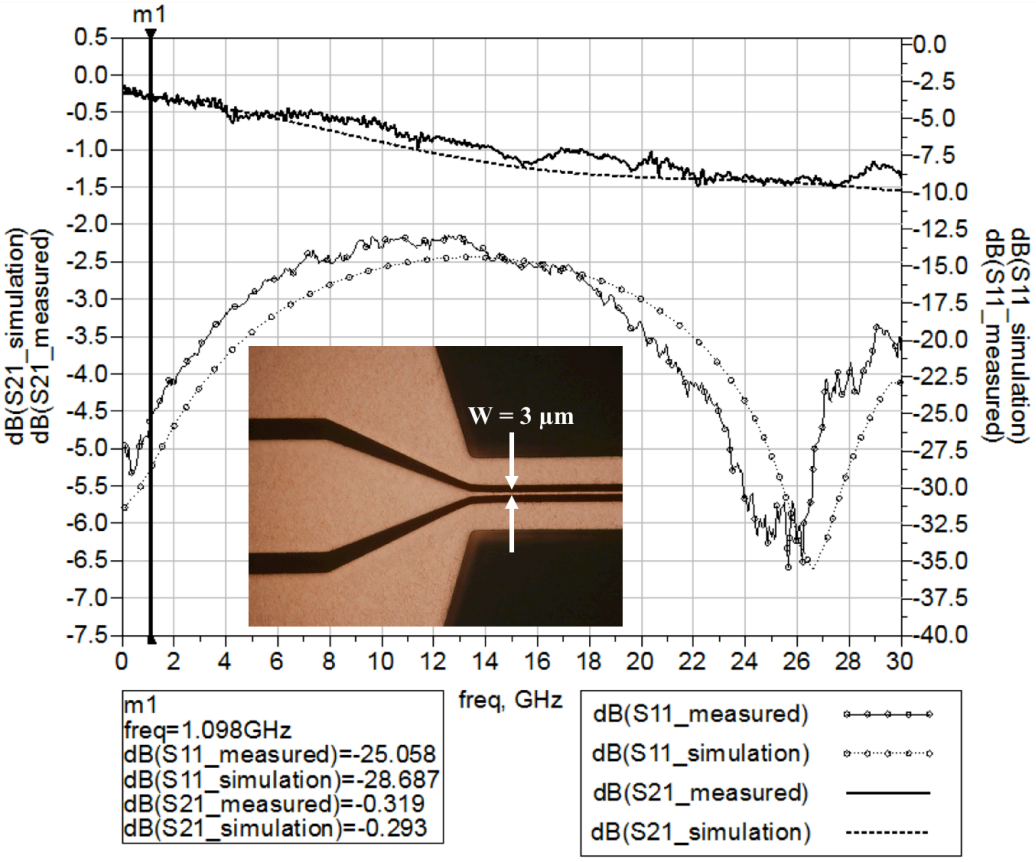


Figure 49. Characterization of W = 3 µm RDL at L = 5 mm.

height variations compared to simulation.

Line performance at 1 GHz is highlighted in each CPW measurement. Return loss below -25 dB was observed for each design which indicated good impedance matching at Z_0 = 50 Ω. More importantly, line attenuation was shown to increase at decreased conductor cross section. Line attenuation 0.04 dB/mm was observed for W = 5 um compared to 0.06 dB/mm for W = 3 um. Specifically, a decrease in conductor cross section by approximately 50% increased line attenuation by roughly 33% at 1 GHz. Both designs, however, demonstrated lower loss than BEOL wide I/O interconnects. Silicon interposer BEOL RDL -3dB bandwidth was shown to be approximately 2.2 GHz [31]. High frequency characterization of the RDL geometries on the glass interposer test vehicle indicated a -3dB beyond 30 GHz.

3.2.3.2 Interconnect Delay Simulation

Interconnect delay of fine pitch test structures was compared to BEOL silicon interposers. The BEOL silicon interconnect model used a lumped element approximation with silicon line resistance R_{Si} = 32.5 Ω and capacitance C_{Si} = 1.25 pF. These values are consistent with those used for the design of a BEOL silicon interposer and were extrapolated for L = 5 mm [31]. The Thevenin equivalent circuit model used for the wide I/O buffer assumed a linear MOSFET model with an on resistance R_S = 10 Ω. The glass interposer interconnect model used the measured S-parameters discussed in 3.2.3.1.

The step response of the glass interposer interconnect for W = 5 μm and W = 3 μm are shown in Figure 50 and Figure 51 respectively as the dashed line. Parameters for the

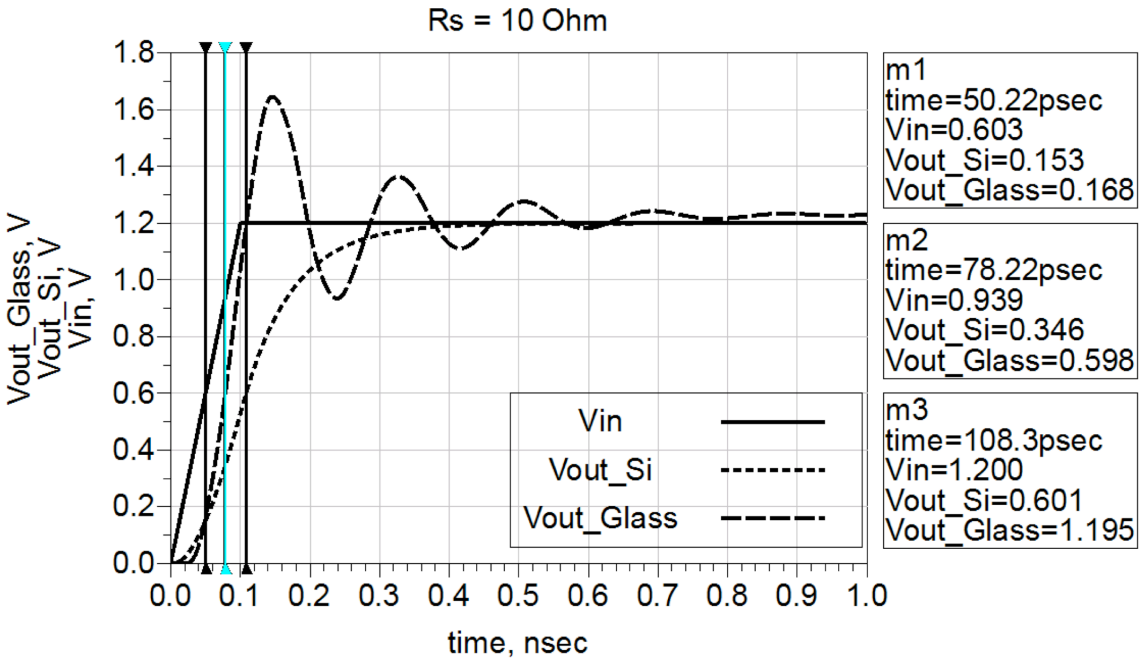


Figure 50. W = 5 µm interconnect delay (dashed line) at L = 5 mm compared to wafer-based silicon (dotted line).

voltage step were in line with 2 Gbps signaling and the HBM specification. Voltage rise time t_r = 0.2 UI = 100 ps was used with a voltage step of V_{IN} = VDDQ = 1.2 V.

Interconnect delay T_d was calculated at V_{OUT} = 0.5 VDD = 0.6 V and expressed as a fraction of the bit unit interval UI = 500 ps at 2 Gbps. The simulated time delay using the measured S-parameter interconnect model was T_{d_Glass} = 0.056 UI and T_{d_Glass} = 0.064 UI for W = 5 µm and W = 3 µm respectively compared to T_{d_Si} = 0.114 UI. Interconnect latency was reduced by up to 50% using fine pitch interconnects with a 5:1 AR.

Transmission line (inductive) behavior dominated for high aspect ratio glass interposer interconnects compared to the highly resistive silicon interposer interconnects. Therefore, interconnect delay was dependent on the transmission line time of flight

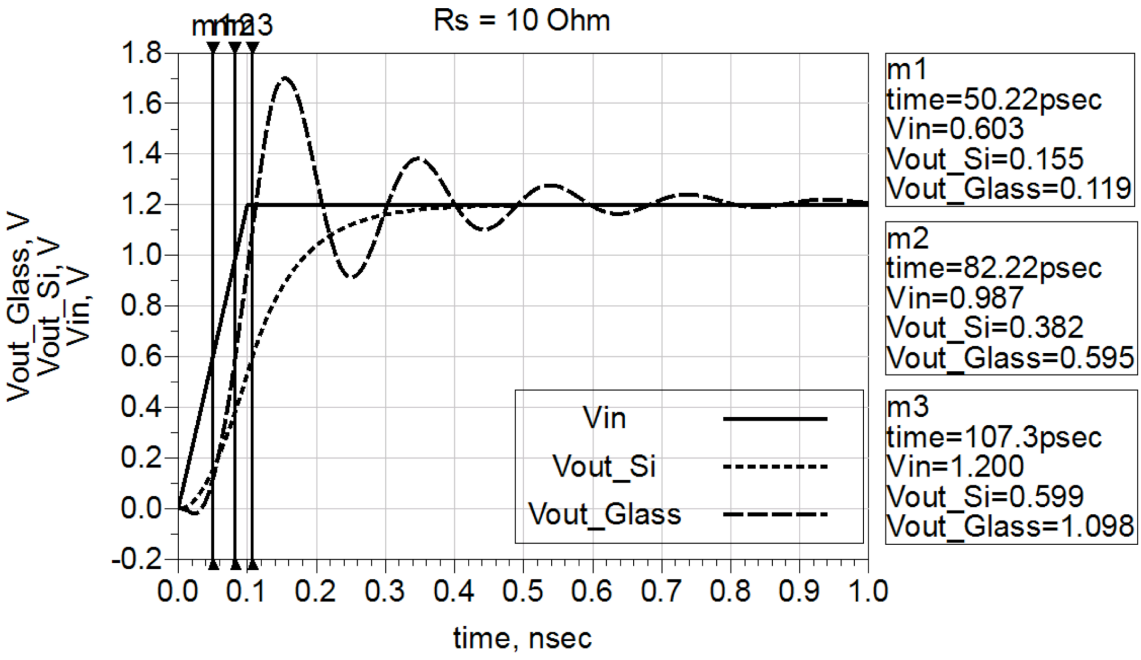


Figure 51. W = 3 µm interconnect delay (dashed line) at L = 5 mm compared to wafer-based silicon (dotted line).

compared to the RC time delay of silicon interposer interconnects. Interconnect latency was reduced using low resistive interconnects, but inductive behavior for $R < 5Z_0$ caused ringing at V_{OUT} and, depending on receiver threshold voltage, may cause glitches. Therefore, in-line termination at the output buffer was used to reduce ringing. The step response for R_{S_Glass} = 25 Ω is compared to the step response for R_{S_Si} = 10 Ω in Figure 52 and Figure 53 for W = 5 µm and W = 3 µm respectively.

The source resistance for the silicon interposer was assumed given MOSFET on resistance and on-chip interconnect resistance for a CMOS buffer. The termination resistance for a glass interposer wide I/O interconnect was swept between R_S = 10 – 50 Ω. Ringing at the receiver approached a capacitive RC behavior with increased source

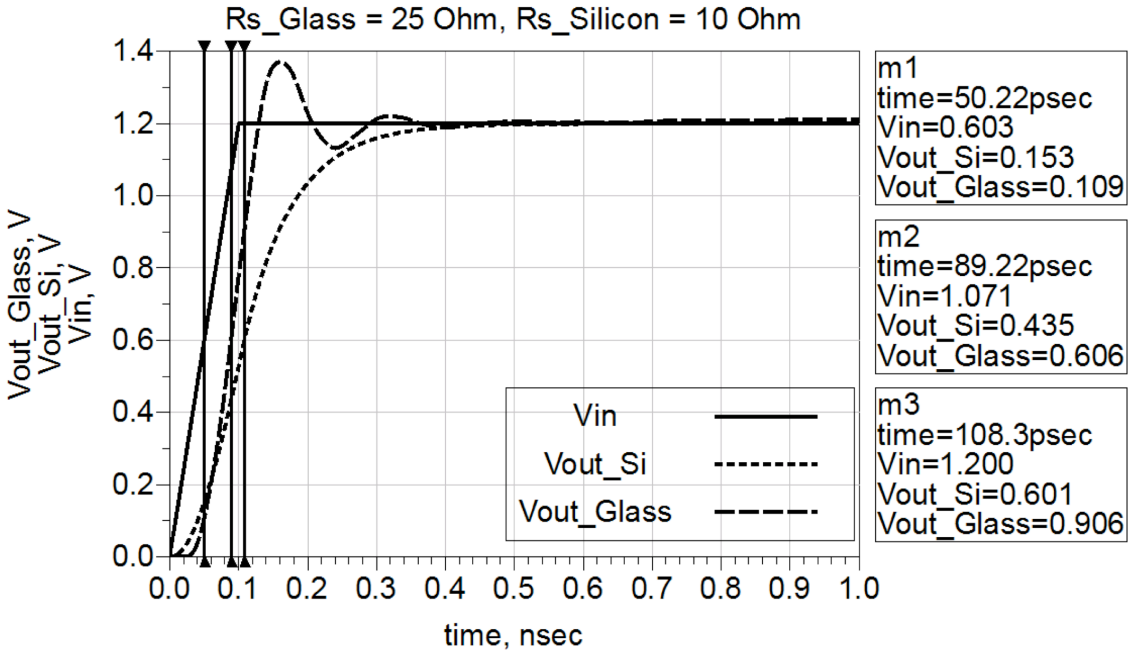


Figure 52. W = 5 µm interconnect delay at L = 5 mm with source termination.

impedance. Source termination $R_S = Z_0/2$ was shown to reduce the ringing envelope such that the settling time was less than the RC response of the silicon interposer wide I/O interconnect. At $R_S = Z_0/2$ (25 Ω for 50 Ω CPW test structure), the interconnect delay was T_{d_Glass} = 0.078 UI and T_{d_Glass} = 0.086 UI for W = 5 µm and W = 3 µm respectively compared to T_{d_Si} = 0.114 UI. Interconnect delay was reduced by up to 30% using high aspect ratio wide I/O interconnects on the glass interposer with in-line source termination compared to a BEOL silicon interposer. The increased delay compared to results in Figure 50 and Figure 51 was due to increased RC delay at the buffer.

Wide I/O interconnect latency was reduced compared to BEOL silicon interposer by increasing conductor cross section. Increased conductor cross section, however, led to transmission line behavior dominating RC line behavior, which was observed for BEOL

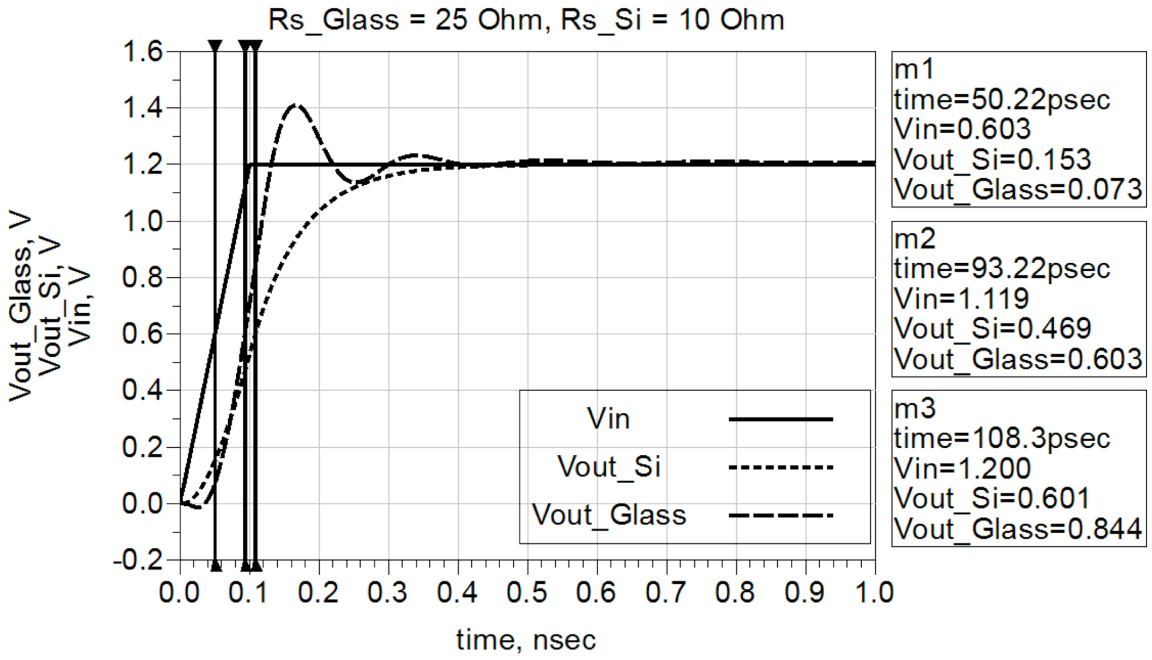


Figure 53. W = 3 µm interconnect delay at L = 5 mm with source termination.

wide I/O interconnects. Source termination $R_S = Z_0/2$ was shown to be an optimal point to reduce ringing and latency. Using this topology, interconnect delay was compared at different line cross section. Fabrication results showed that copper height to line width ratios up to 5:1 were achieved using panel processes. This resulted in a fabricated conductor cross section of A_{fab} = 42 µm^2 ($W_{fab} \approx$ 4.2 µm) and A_{fab} = 22 µm^2 ($W_{fab} \approx$ 2.2 µm). The fabricated line width W_{fab} was reduced due to 0.4 µm overetching using a SAP compared to the design line width W. Wide I/O latency for a glass interposer was compared in Figure 54 at these fabricated conductor cross sections.

Line delay per unit length t_d was reduced as a result of increased conductor cross section and consistent with results in Figure 35. Interconnect delay $t_{d\_3\mu m}$ = 1.76 x 10^{-2} UI/mm (2 Gbps at L = 5 mm) was observed for the minimum fabricated line width of 2.2

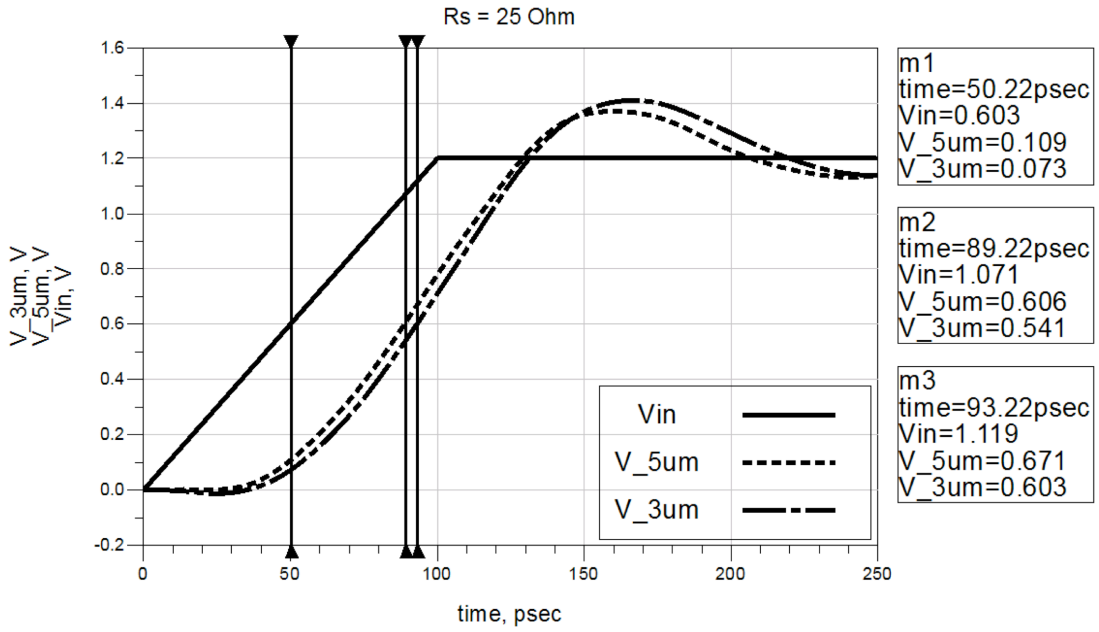


Figure 54. Wide I/O latency compared at various line cross section at *L* = 5 mm.

µm compared to $t_{d\_5\mu m}$ = 1.56 x 10^{-2} UI/mm (2 Gbps at *L* = 5 mm) for a fabricated line width of 4.2 µm. As shown previously, both implementations exhibited a lower line latency when compared to wafer-based silicon interposer t_{d_Si} = 2.0 x 10^{-2} UI at 2 Gbps, and are consistent with wide I/O electrical performance objectives summarized in Table 2.

3.3 Summary

The modeling and design of low latency wide I/O established a roadmap for panel-based fabrication of 2.5-D glass interposer packages. Wide I/O latency was shown to decrease with increasing copper thickness to signal width *AR*. Furthermore, interconnect

delay per unit length was shown to vary indirectly with $\sqrt[5]{A}$, where A was the conductor cross section, and A greater than 5 μm^2 was required to reduce wide I/O latency below BEOL silicon interposer.

Die-to-die interconnect density for wide I/O was shown to depend on RDL geometry including line pitch, line width, and microvia padstack diameter. A roadmap for RDL scaling was provided to achieve interconnect density δ = 450 lines/mm at 2 μm RDL pitch. Scaling microvia padstack below 10 μm was identified as a key enabling technology for a 2.5-D glass interposer package. At this diameter, die escape and fan-out RDL geometry was matched and conductor cross section was constant for die-to-die channels.

The effect of crosstalk on wide I/O latency was studied and showed that copper height must be optimized to maintain line performance. It was recommended to scale ILD thickness below 5 μm to increase ground coupling and reduce the effect of crosstalk on signal latency. An alternative design solution to include guard traces for wide I/O was recommended to address potential manufacturability challenges associated with thin film polymer thickness below 5 μm.

CHAPTER 4. MODELING, DESIGN, FABRICATION AND CHARACTERIZATION OF RDL FOR EXTERNAL I/O

This chapter describes the research on the design and demonstration of high speed channels on glass interposers, as shown in Figure 55. A distinct advantage of using glass as an interposer and package substrate material is its low permittivity (ε_r = 5.4 @ 20 GHz) and low loss tangent ($tan\delta$ = 0.005 @ 20 GHz), when compared to silicon. The high conductor and dielectric losses of RDL on silicon interposers limited the electrical performance of external I/O connections from interposer to system. The electrical performance of external I/O for the glass interposer package was improved further by implementing high speed RDL transmission lines directly on the glass surface. This design choice was made to leverage the low surface roughness (Ra < 5 nm) and low loss factor of glass to reduce conductor and dielectric losses respectively to improve attenuation compared to silicon.

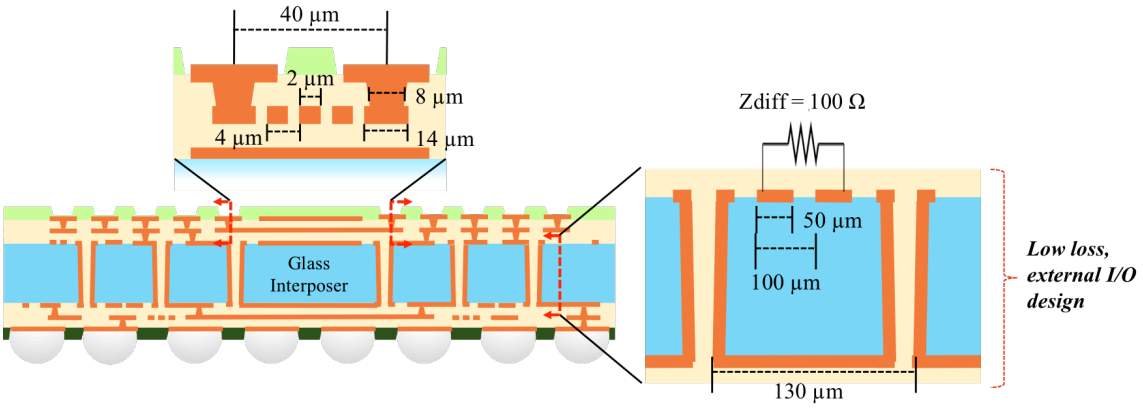


Figure 55. 2.5-D glass interposer with high speed external I/O on glass.

Differential signaling has been the preferred choice for external I/O in high performance computing systems. The advantages of differential signaling include [50]:

- Low PDN noise—ground bounce and rail collapse.
- Low vulnerability to crosstalk and return path discontinuity.
- Low susceptibility to switching noise at connectors and package interconnections.
- High differential amplifier gain.

Therefore, this signal topology is typically used for high speed serial interfaces including Serializer/Deserializer (SerDes) and Peripheral Component Interconnect Express (PCI-e) bus standards for FPGA and graphics applications respectively.

The modeling, design, fabrication and characterization of RDL on glass interposers for external I/O is described below. First, transmission line attenuation for an isolated differential channel was simulated for RDL traces fabricated directly on the glass surface.

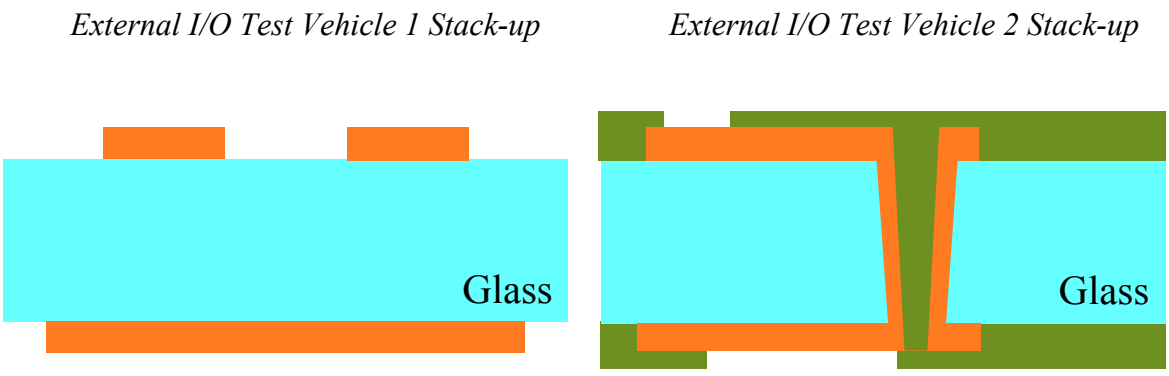


Figure 56. External I/O RDL test vehicle stack-ups.

The crosstalk between differential pairs was then simulated and included the effect of a sequential build-up polymer dielectric layer on transmission line performance. Therefore, two glass test vehicle stack-ups were considered for the fabrication and characterization as shown in Figure 56.

4.1 External I/O RDL on Bare Glass

The purpose of this test vehicle was to determine the attenuation of a differential pair up to 14 GHz, and to study the effect of bend radius on differential insertion loss. External I/O channels typically conform to strict insertion loss masks defined in various design guidance specifications. Channel length budgets that meet these loss masks are developed based on an established loss per unit length design rule to reduce design time. The SAP used for the fabrication of the glass interposer package did not impose limits for traces to maintain 45-degree routing and meandering structures similar to PWB were achieved. A minimum transmission line bend radius was required to maintain line impedance and to reduce insertion losses at these junctions for high speed channel design.

The design flow for high speed RDL on glass is summarized in Figure 57. The design assumed a 130 μm glass thickness and 5 μm copper trace height. The electrical properties of glass listed in Table 6 and a copper conductivity of 5.8×10^7 S/m were used in simulation.

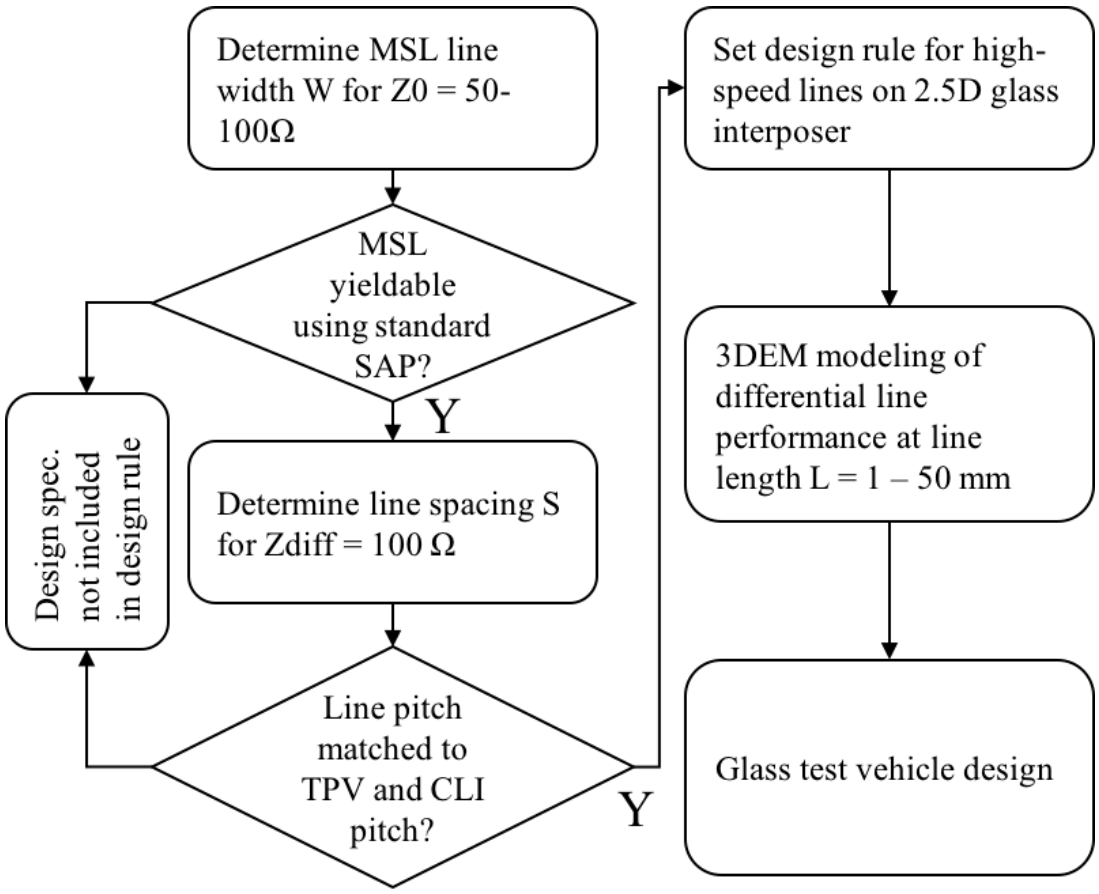


Figure 57. External I/O design process flow.

The first design step determined the line width W of an isolated microstrip line (MSL) to achieve Z_0 = 50 – 100 Ω on a glass substrate. The minimum RDL trace width and space on glass was assumed to be W_{min} = 20 µm and S_{min} = 20 µm. This assumption was made to guarantee line yield with good line width control using SAP, and to increase minimum line cross section to 100 µm^2. A 2D-EM simulation was then used to determine line spacing S between two MSLs to achieve a differential impedance Z_{diff} = 100 Ω. The results of this analysis are shown in Figure 58. For each MSL variation, the line spacing was swept from S = 200 µm down to S_{min} = 20 µm and Z_{diff} was extracted.

Table 6. Glass electrical properties [51].

Frequency [GHz]	ε_r	$tan\delta$
3.1	5.3775	0.0051
6.3	5.1968	0.0051
9.4	5.2561	0.0053
12.5	5.2861	0.0056
15.6	5.3042	0.0058
18.6	5.3775	0.0049
21.7	5.3775	0.0054
24.7	5.4241	0.0046
27.6	5.5030	0.0063
30.7	5.4902	0.0056
33.6	5.5496	0.0055
36.5	5.5998	0.0055
39.5	5.6123	0.0079
44.6	5.6299	0.0063
49.3	5.6931	0.0084

The design space for differential signaling was large compared to single-ended signaling. Five line and pitch configurations studied in Figure 58 complied with SAP and Z_{diff} = 100 Ω design rules, and were down-selected based on the fan-out routing requirements for the target CLI bump pitch and TPV pitch. Matching differential line pitch to bump pitch and TPV pitch minimized differential impedance mismatch at these interfaces by reducing fan-out length to improve the differential signal integrity. Excessive fan-out length can lead to signal reflection and distortion, ultimately resulting in common mode conversion [50]. A CLI bump pitch D = 150 – 300 μm was assumed for

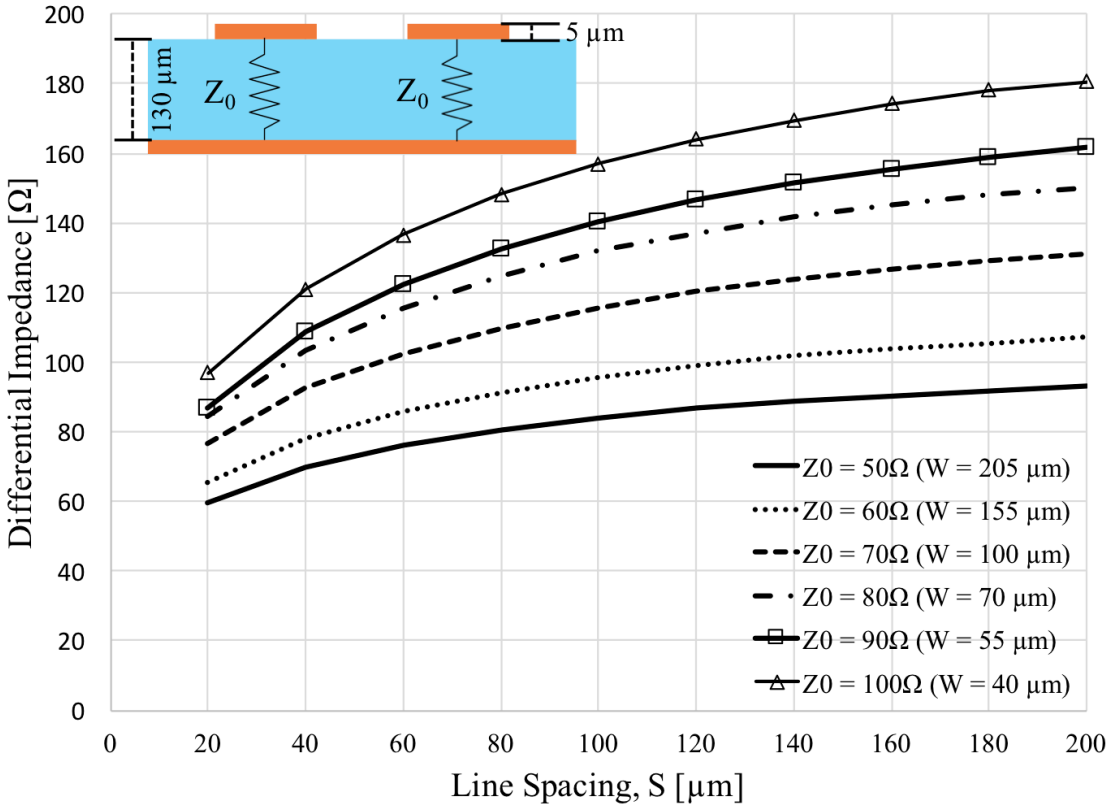


Figure 58. Differential line impedance determined by 2D-EM simulation.

external I/Os. This signal interface typically used a coarser bump pitch compared to wide I/O to reduce crosstalk and achieve higher data rates per channel. Through package via pitch less than *D* was assumed based on fabrication results given in [52]. Therefore, the TPV pitch can match the CLI pitch, which determined the final differential pair spacing. Two designs were selected from the design space to match line pitch (*P*) to chip-level bump pitch as listed below:

1. W = 155 µm for P = 275 µm (Z_0 = 60Ω).

2. W = 100 µm for P = 154 µm (Z_0 = 70Ω).

Differential return loss S_{DD11} and differential insertion loss S_{DD21} were modeled using 3D-EM simulations to analyze the line performance. Figure 59 and Figure 60 shows the differential return loss for design variation (1) and design variation (2) respectively. The models used to simulate differential line performance are shown as superimposed images in Figure 59 and Figure 60. Port sizing for each design variation was optimized based on ANSYS™ port sizing recommendations. The simulated differential return loss showed good broadband matching for each design variation up to 40 GHz. Design variation (1) resulted in less return loss with a S_{DD11_max} = -18 dB, while design variation (2) resulted in S_{DD11_max} = -15 dB.

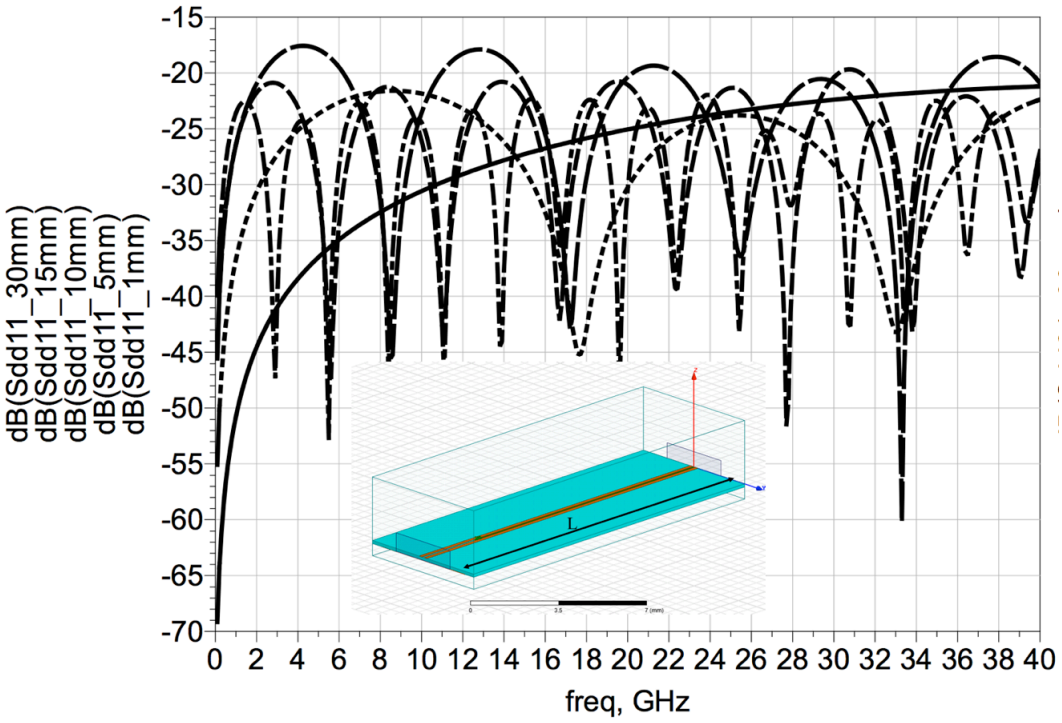


Figure 59. Differential return loss (W = 155 µm, P = 275 µm).

The simulated differential insertion losses for design variations (1) and (2) are shown in Figure 61 and Figure 62 respectively for line lengths L = 1 – 30 mm. The average line attenuation for each design variation was comparable—α_1 = 0.03 dB/mm and α_2 = 0.04 dB/mm at 14 GHz. The performance difference was attributed to the increased conductor losses at decreased line widths, which was exaggerated at high frequencies due to smaller skin depths. Compared to wafer-based silicon interposers, however, the line attenuation for differential RDL on glass was approximately 10x lower [43].

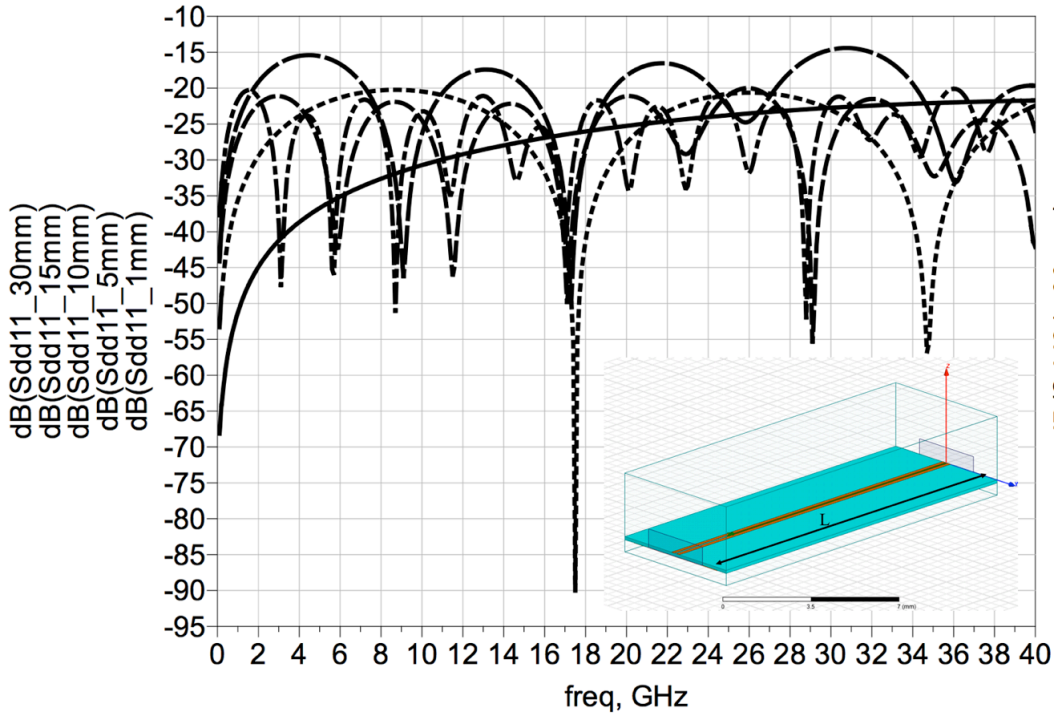


Figure 60. Differential return loss (W = 100 µm, P = 154 µm).

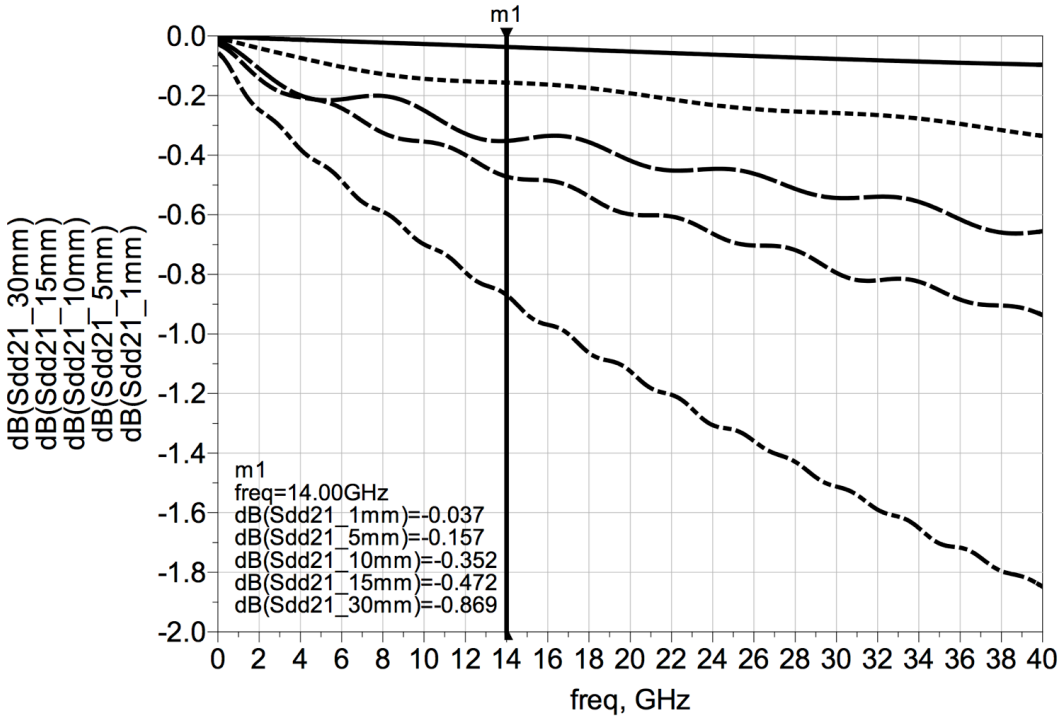


Figure 61. Differential insertion loss (W = 155 µm, P = 275 µm).

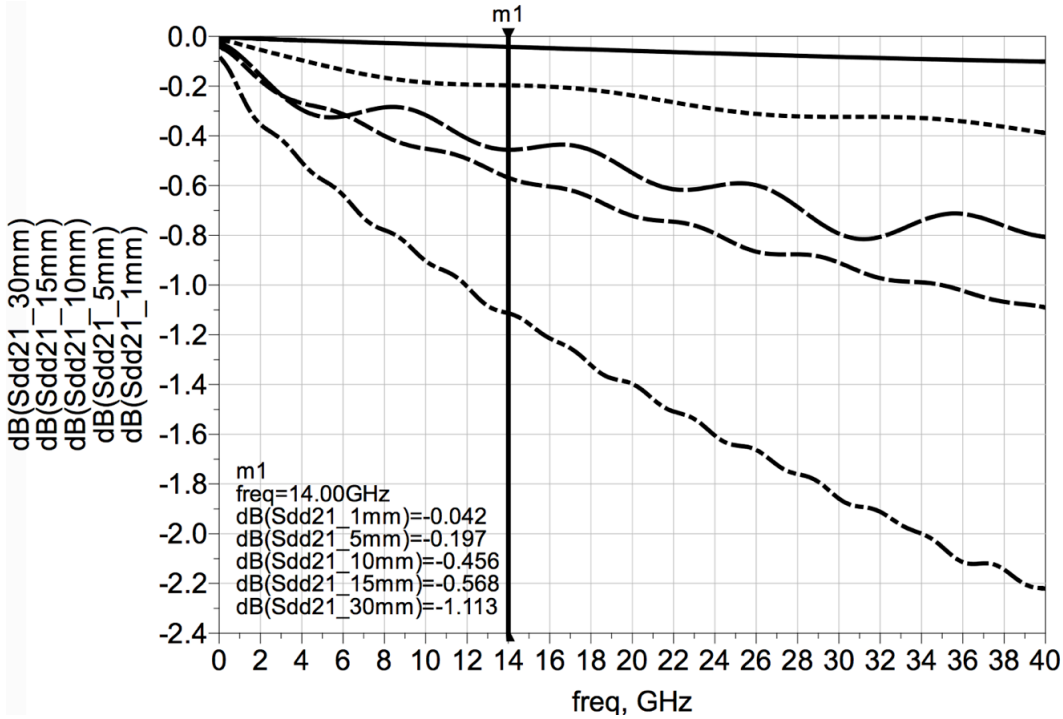


Figure 62. Differential insertion loss (W = 100 µm, P = 154 µm).

4.1.1 Process Dependent Losses

Simulated insertion loss for differential pair design variations (1) and (2) showed that transmission lines on glass had significantly lower attenuation compared to silicon, but also highlighted the importance of skin effect losses for high speed channels. The skin effect was expected to increase differential insertion losses due to the titanium seed layer and the lower electrical conductivity of titanium compared to copper. Fabricating RDL directly on glass by SAP necessitated the use of a titanium-copper seed layer to improve copper to glass adhesion. The simulated differential insertion loss, that

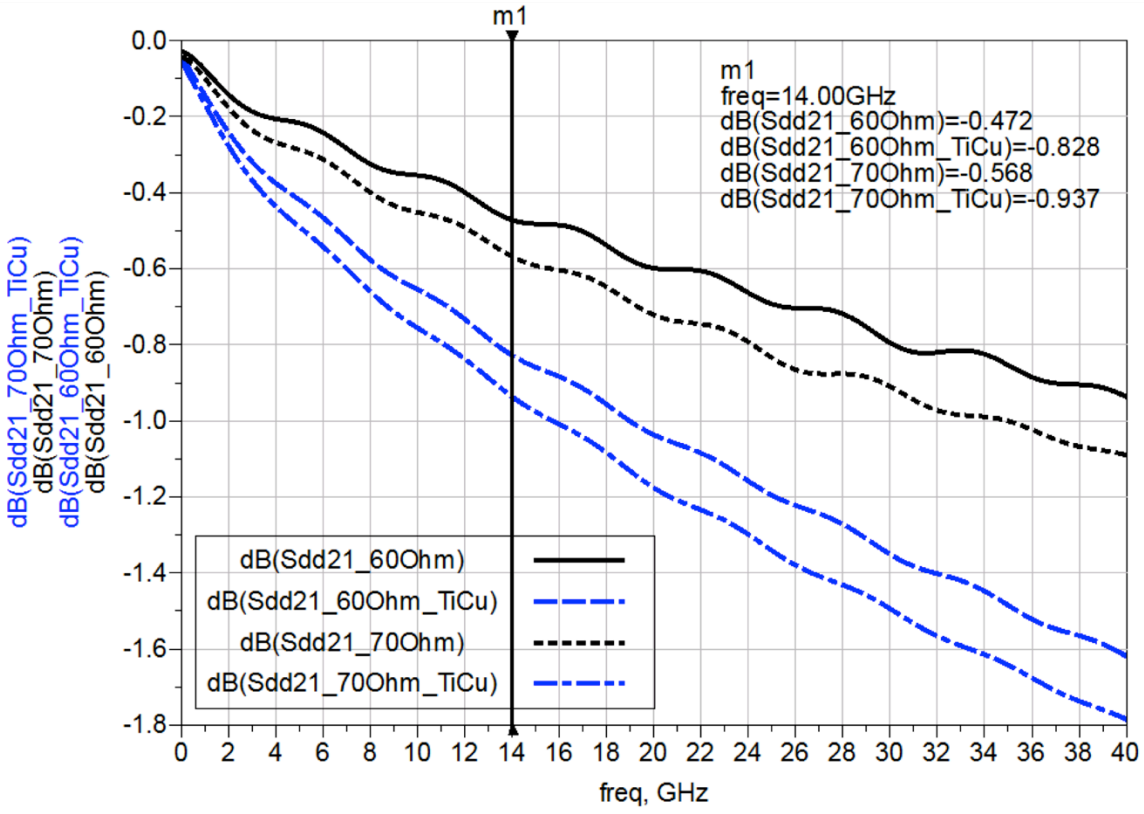


Figure 63. Effect of Ti-Cu SAP seed layer on differential insertion loss (*L* = 15mm).

considered the effect of a titanium seed layer is shown in Figure 63 for L = 15 mm for design variation (1) (black traces) and design variation (2) (blue traces).

Skin effect resulted in a majority of the current flow through the titanium seed layer at high frequency for both the signal and return path based on the MSL stack-up shown in Figure 56. The lower bulk conductivity of titanium σ_{Ti} = 1.82x10^6 S/m compared to copper σ_{Cu} =5.8x10^7 increased line resistance as a result. In general, line attenuation increased by approximately 70% where α_1 = 0.05 dB/mm and α_2 = 0.07 dB/mm at 14 GHz.

4.1.2 Differential Die Breakout Routing

Differential impedance simulation results in Figure 58 showed that line pitch can be matched to CLI or TPV pitch to reduce the effect of impedance discontinuities at these interfaces. This design constraint maintained differential impedance for die breakout, but the effect of turning on channel loss needed to be quantified for external I/O. It was assumed that die breakout routing did not use 45-degree routing. Therefore, the following assumed that line turning was achieved with rounded features at different bend radii where a 90-degree turn was not allowed. The model of a typical turning test structure is shown in the cutout of Figure 64.

Line Attenuation (without considering process dependent losses) was compared in Figure 64 at turning radii R = 0.15, 0.4, 0.8, 1, 2, 4, and 8 mm for design variation (2). This design variation allowed for the tightest turn radius while maintaining line pitch and width for Z_{diff} = 100 Ω. The straight line distance between the turning structures was fixed at λ/4 = 5.35mm (f = 14 GHz). An s-turn type test structure was used to maintain

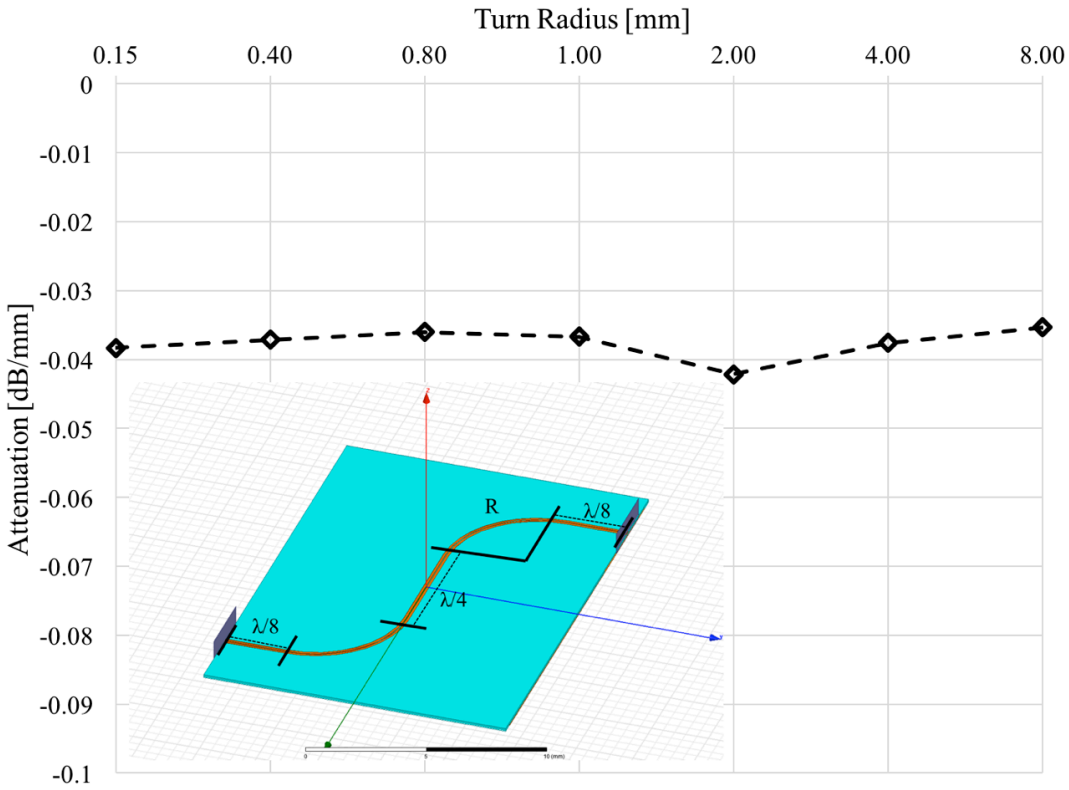


Figure 64. The effect of turn radius on attenuation (*W* = 100 µm, *P* =154 µm).

symmetry of the differential trace. The results of this analysis showed that minimum turn radius R = 0.15 mm did not significantly affect attenuation compared to straight line attenuation shown in Figure 62. Therefore, RDL density at die escape was not affected by turn radius.

4.2 External I/O Crosstalk

The simulation of RDL on glass for low loss external I/O was discussed in 4.1 using stack-up 1 in Figure 56, and showed line attenuation was lowered by up to 10x compared to wafer-based silicon interposers. External I/O in a glass interposer package,

however, must consider the effect of sequential build-up dielectric on channel performance. Specifically, external I/O stack-up 2 in Figure 56 was used to determine differential crosstalk. The build-up dielectric material properties were based on a benzocyclobutene (BCB) photo-imageable dielectric with ε_r = 2.5 and $tan\delta$ = 0.002 at 10 GHz.

Line pitch and width was adjusted to maintain Z_{diff}=100 Ω using the same design flow given in Figure 57. The extracted differential impedance for line space S = 20 – 600 µm at line widths to achieve Z_0 = 50 – 100 Ω is shown in Figure 65. The design assumed

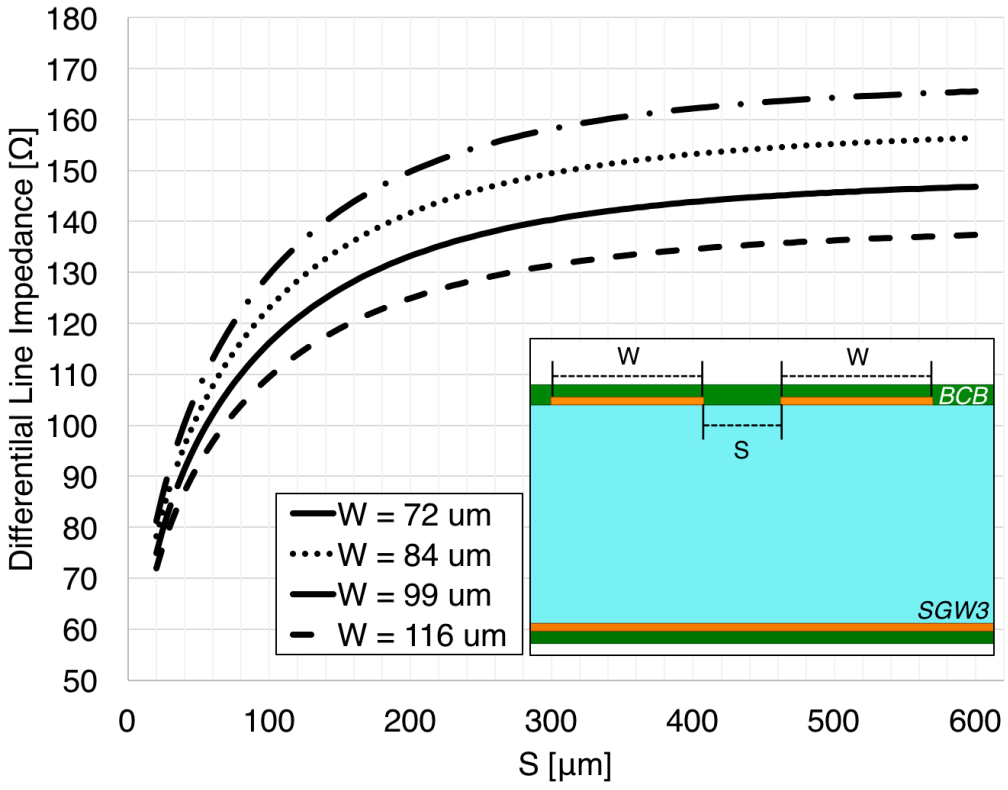


Figure 65. Differential line impedance with build-up dielectric determined by 2D-EM simulation.

thicknesses of 140 µm for glass, 10 µm for BCB, and 5 µm for copper. The effect of increased glass thickness, and the build-up dielectric on differential impedance was minimal compared to design variation (2) in 4.1, and one design variation W = 100 µm at P = 150 µm was used for crosstalk analysis.

The differential crosstalk was expected to be higher due to weaker ground coupling compared to implementations in thinner build-up dielectric layers. Four crosstalk test structures without ground shielding were included in the test vehicle design with variable differential pair spacing pS ranging from pS = 50 – 400 µm as shown in Figure 66. Ground shielding was not introduced in these test structures since the main purpose was to determine a minimum pair spacing design rule to meet broadband crosstalk requirements up to 40 GHz.

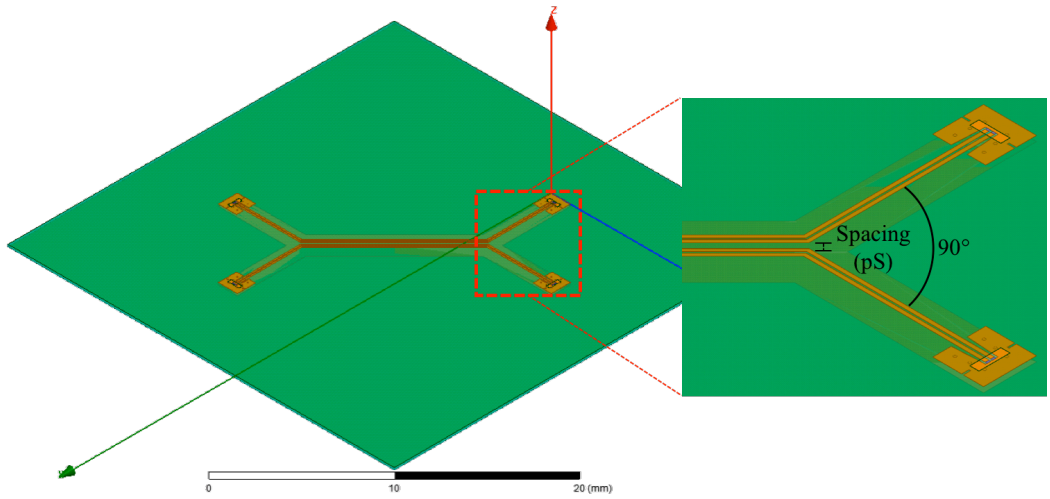


Figure 66. 3D-EM crosstalk model with variable pair spacing *pS*.

Crosstalk between differential MSL pairs was simulated using ANSYS™ Electronic Desktop, and Figure 66 shows the model geometry used in the simulation. Signal excitation used lumped ports assigned to a ground-signal-signal-ground differential launch pad. Near-end and far-end crosstalk were simulated at the aforementioned differential pair spacing range. The simulation results are shown in Figure 67 and Figure 68 for near- and far-end differential crosstalk respectively. As expected, crosstalk improved with increased pair spacing and near-end crosstalk was greater than far-end crosstalk across the frequency range of interest. More importantly,

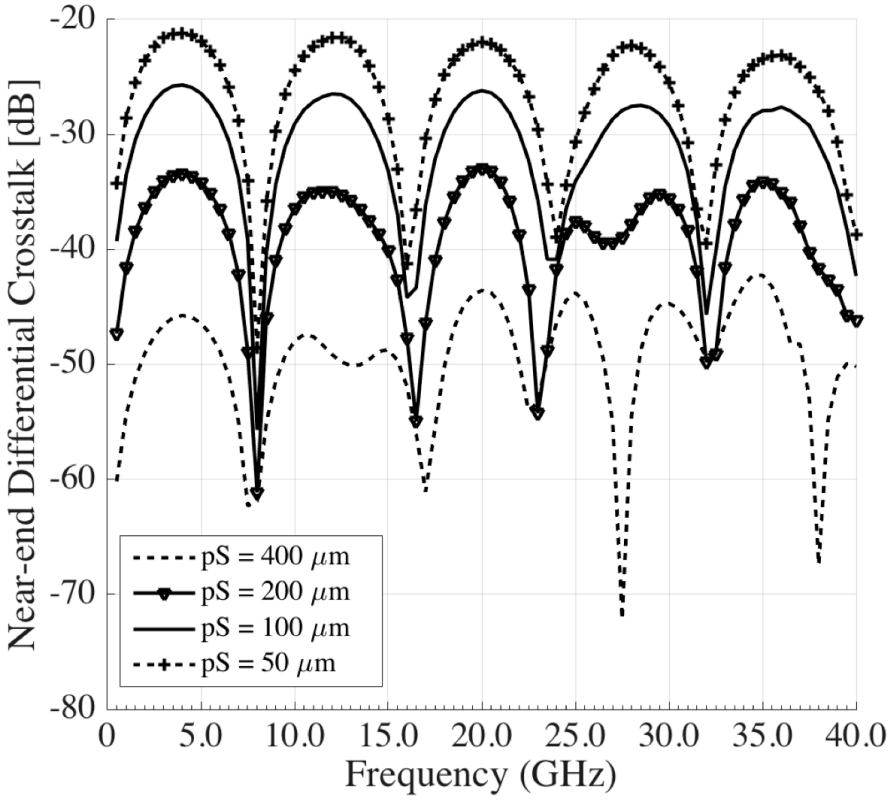


Figure 67. Near-end differential crosstalk for *pS* = 50 – 400 µm.

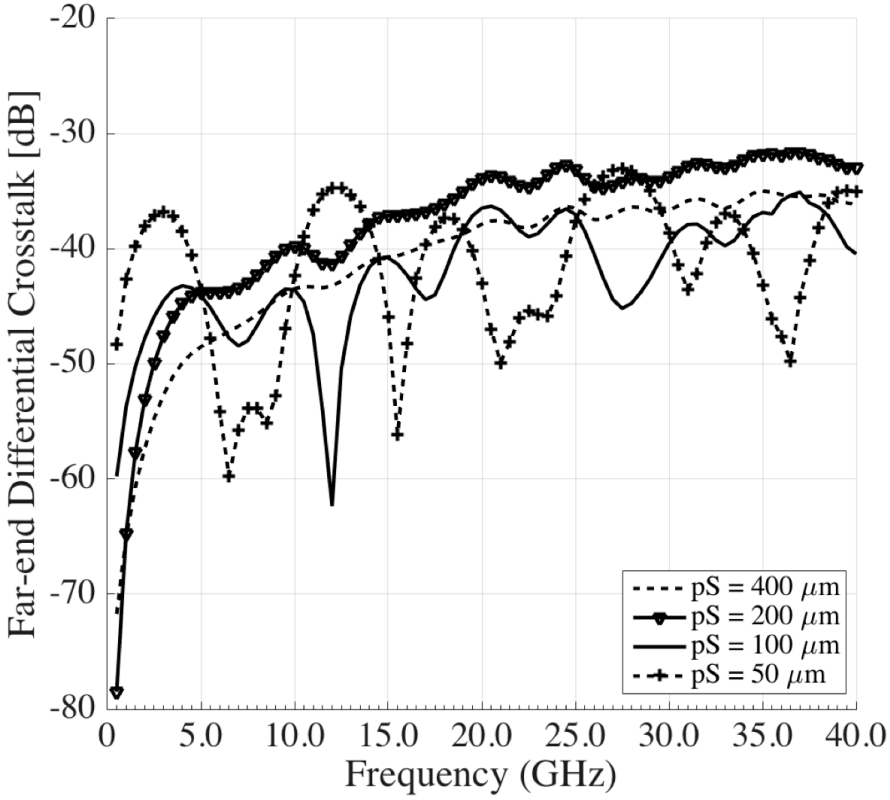


Figure 68. Far-end differential crosstalk for *pS* = 50 – 400 µm.

these simulation results indicated that a differential crosstalk less than -30 dB was expected when pair spacing was greater than 200 µm up to 40 GHz without ground shielding.

4.3 Design and Characterization of Low Loss RDL for External I/O

This section discusses the design, fabrication and characterization of high frequency RDL test structures in two glass test vehicles. Test vehicle 1 was used to characterize the attenuation of RDL on glass for the two differential line and pitch variations discussed in 4.1 at interconnect lengths up to 50 mm. Test Vehicle 2 was used

to characterize crosstalk between differential pairs at interconnect lengths up to 10 mm, and study the effect of TPVs on external I/O performance.

4.3.1 External I/O RDL Test Vehicle 1

The primary focus of this test vehicle was the process demonstration and characterization of RDL fabricated directly on glass. Test vehicle 1 used the two-metal layer design rule shown in Figure 69 fabricated on a 76.2 mm x 76.2 mm x 130 µm glass panel. The via-first glass panels were provided by Corning Inc. with a TPV pattern at 60 µm diameter and 120 µm pitch.

Through package via pitch was not a critical design parameter for the structures included in the test vehicle design shown in Figure 70. Each test structure used an array of vias to provide a signal return path and signal via transitions were not considered for characterization. High frequency test structures included: straight-line differential traces

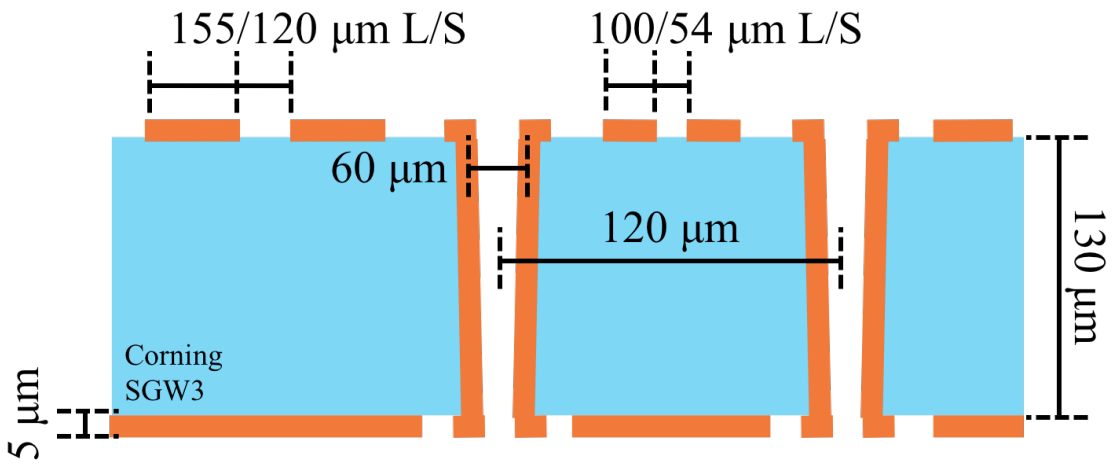


Figure 69. External I/O Test Vehicle 1 design rule.

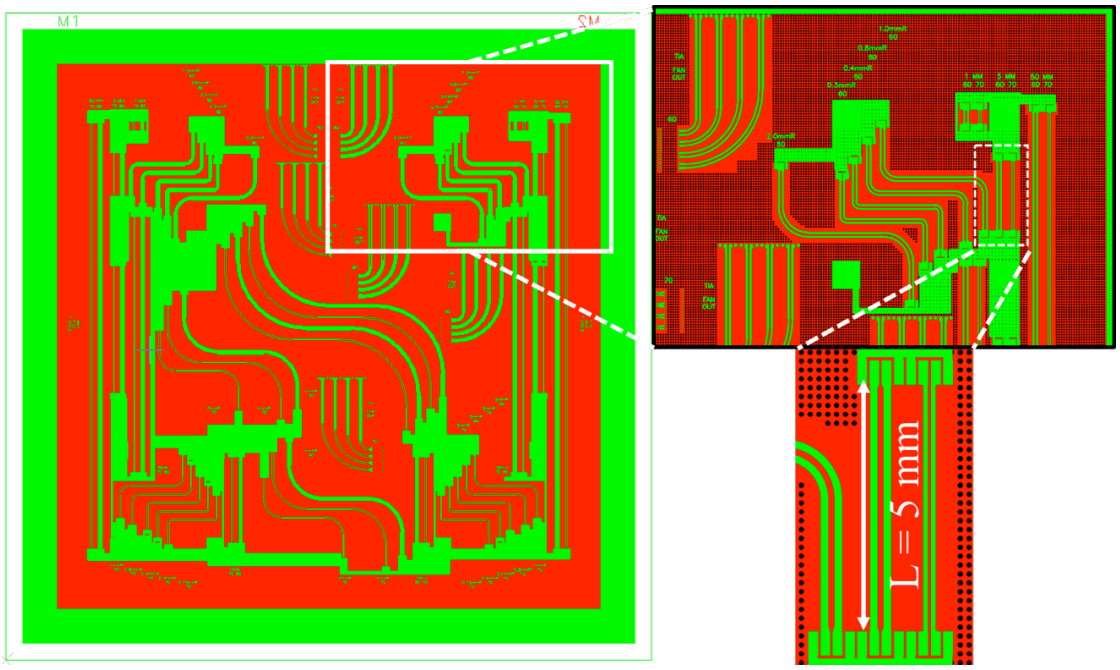


Figure 70. External I/O Test Vehicle 1 two-metal layer layout.

at L = 1, 5, 10, 15, 30, and 50 mm; turning differential traces at bend radii R = 0.3, 0.4, 0.8, 1, 2, 4, and 8 mm; and fan-out structures for a commercial-off-the-shelf trans-impedance amplifier with 150 μm chip-level bump pitch.

The glass test vehicle fabrication used a panel-scalable process flow summarized in Figure 71 to form two-metal layers on bare glass using a single SAP. A Ti-Cu seed layer was sputtered on glass samples with pre-drilled TPVs. The titanium was used as an adhesion layer between the bare glass and copper metallization, while the copper seed layer thickness was optimized for uniform conductivity during subsequent electrolytic plating.

The total sputtering time for titanium and copper was t = 20 min and t = 40 min respectively, resulting in a 100 nm thick titanium seed layer and 500 nm thick copper

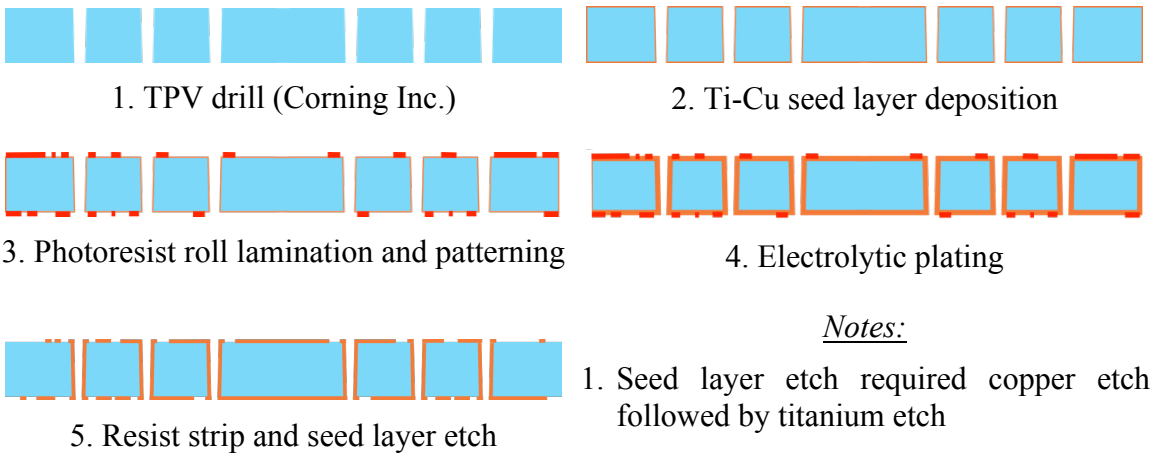
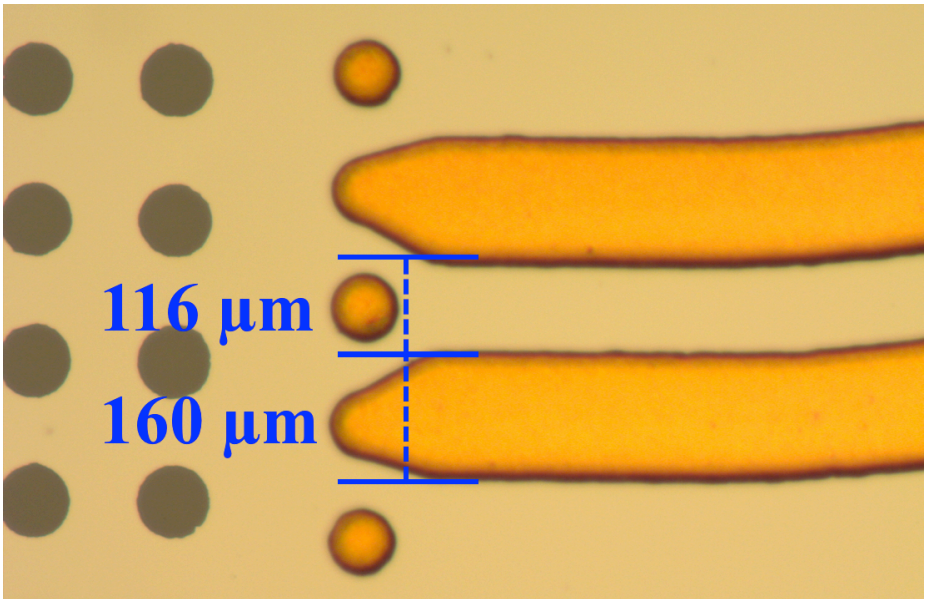


Figure 71. RDL on glass double-sided panel process flow.

seed layer. After seed layer deposition, 15 μm thick dry film photoresist (DFR) was roll laminated at T = 115°C on both sides of the glass. Contact lithography at an exposure time of t = 5.0 s was used for DFR patterning. Electrolytic plating with I = 5.7A for t = 18 min was used to deposit approximately 5 μm of copper and form the signal and ground layers after which the DFR was stripped and seed layers were etched. A hydrofluoric acid flash etch (t = 10 – 20 s) was used to remove the titanium layer.

Fabrication results are shown in Figure 72 for differential pair design variations (1) and (2) in the top and bottom micrographs respectively. The fabricated line width and pitch for design variation (1) was W = 160 μm and P = 276 μm. The fabricated line width and pitch for design variation (2) was W = 102 μm and P = 152 μm. Fabricated line pitch and width varied less than 5% compared to mask dimension. Maintaining line pitch and width is critical for Z_{diff} = 100 Ω, and these variations were attributed to mask fabrication tolerance, mylar mask expansion during exposure, or less than optimized exposure dosage. Therefore, these process induced variations in differential pair line pitch and

(1) W = 155 µm, P = 275 µm



(2) W = 100 µm, P = 154 µm

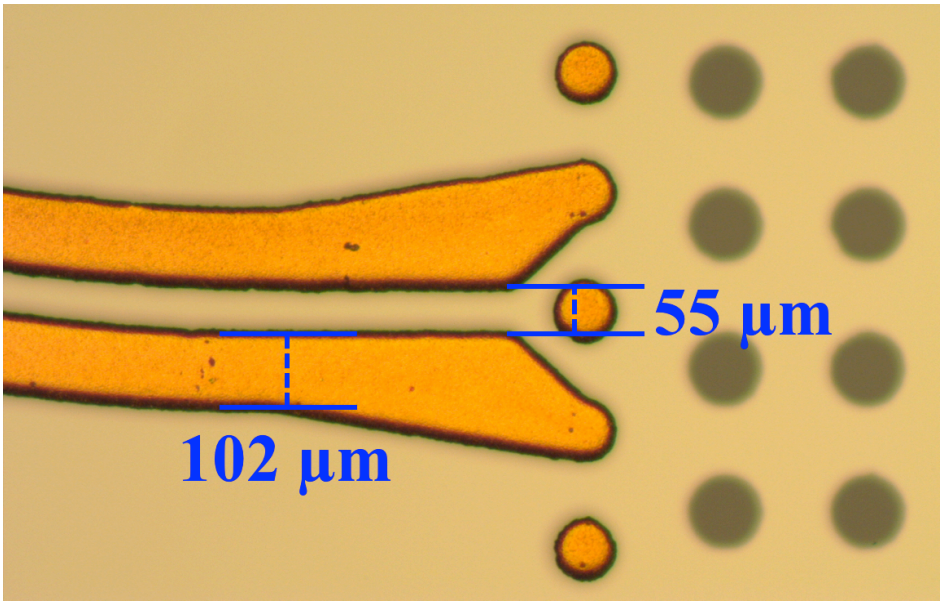


Figure 72. Fabricated differential pairs on glass.

width can be addressed by using a glass mask and further process optimization. Figure 73 shows a cross-section of design variation (2). Contact profilometry was used to measure

an average copper thickness of 8 µm across the panel. Variation in copper thickness was observed, with a minimum measured copper thickness of 5.6 µm. Increased copper thickness and thickness variation was attributed to the electrolytic plating time and can be further optimized based on plating current and mask design.

High frequency characterization was completed using a four port Agilent N5245-90001 Performance Network Analyzer (PNA) with a short-open-load-thru (SOLT) calibration performed on a 129-247 Impedance Standard Substrate using ACP50-D-GSSG-250 probes manufactured by Cascade Microtech. Test structures were measured from 0.1 GHz up to 24 GHz at a 0.1 GHz step size. Measured differential insertion loss is compared to simulation in Figure 74. Good model to hardware correlation was observed up to 22 GHz when considering the effect of titanium seed layer resistivity on insertion

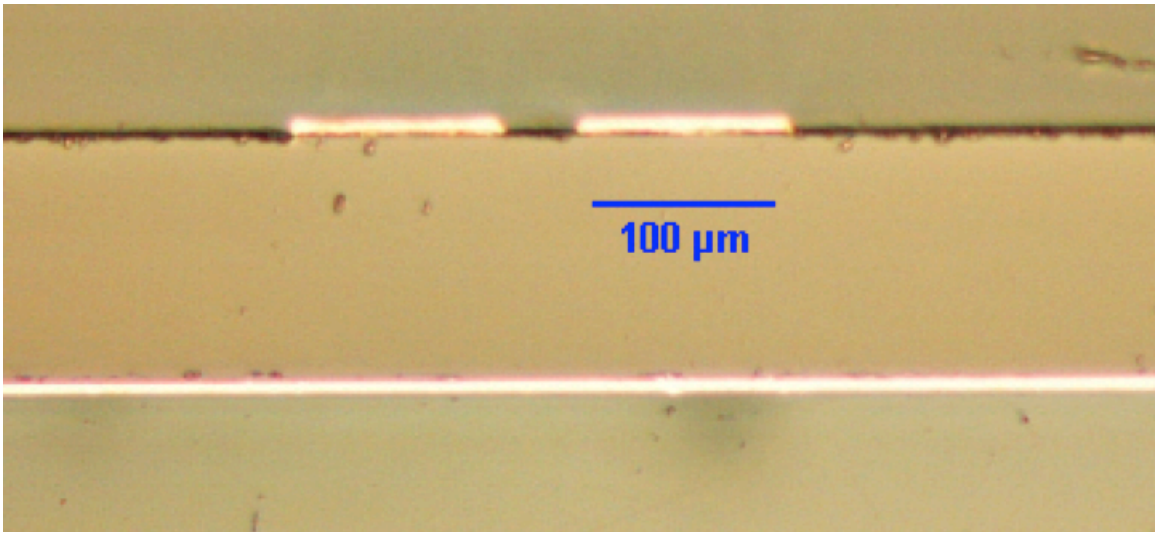


Figure 73. Cross section of fabricated MSL differential pair (W = 100 µm, P = 154 µm).

loss as discussed in 4.1.1.

Figure 75 shows the line attenuation at 14 GHz for transmission line lengths L = 5 – 30 mm. Due to the noise in the measured results, a second order polynomial regression was used to fit the measured data. Then, the fitted loss at 14 GHz was extracted. This fitted parameter for the various line lengths of interest is shown as dots in Figure 75. A linear regression was then applied where the slope of this linear regression represented line loss in decibel per unit length (dB/mm). Attenuation from -0.05 dB/mm up to -0.07 dB/mm at 14 GHz was observed for the differential line variations studied,

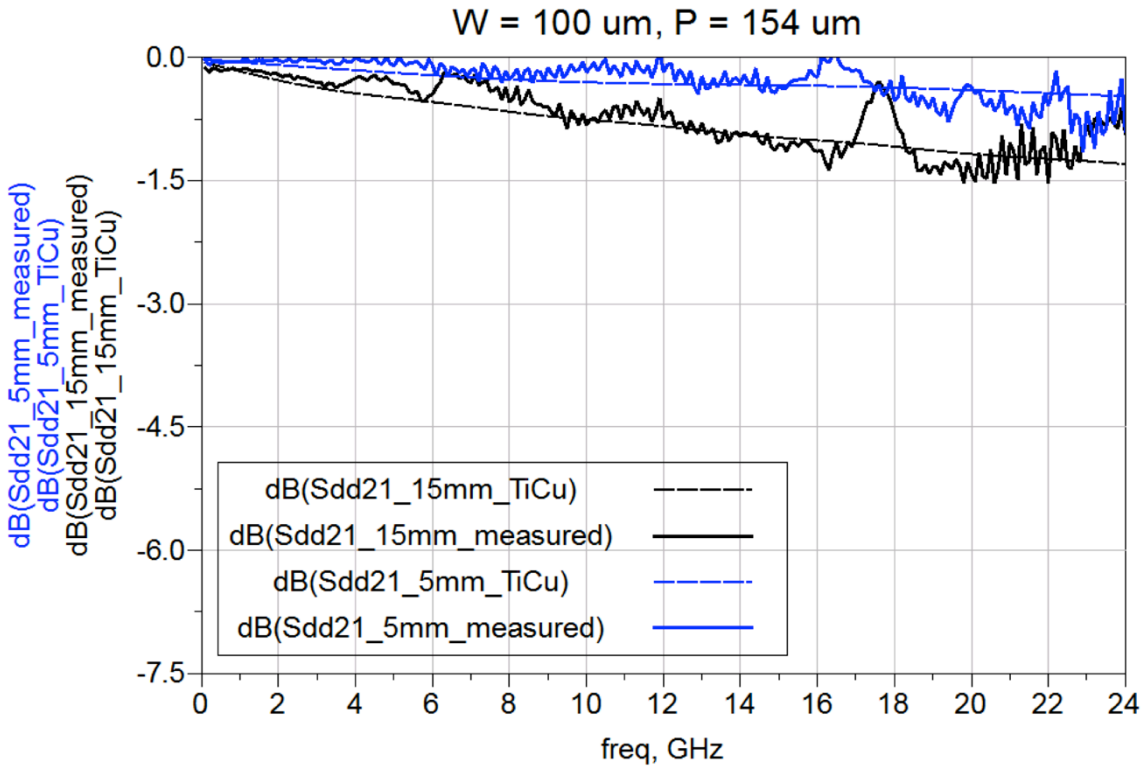


Figure 74. Measured versus simulated differential insertion loss up to 24 GHz.

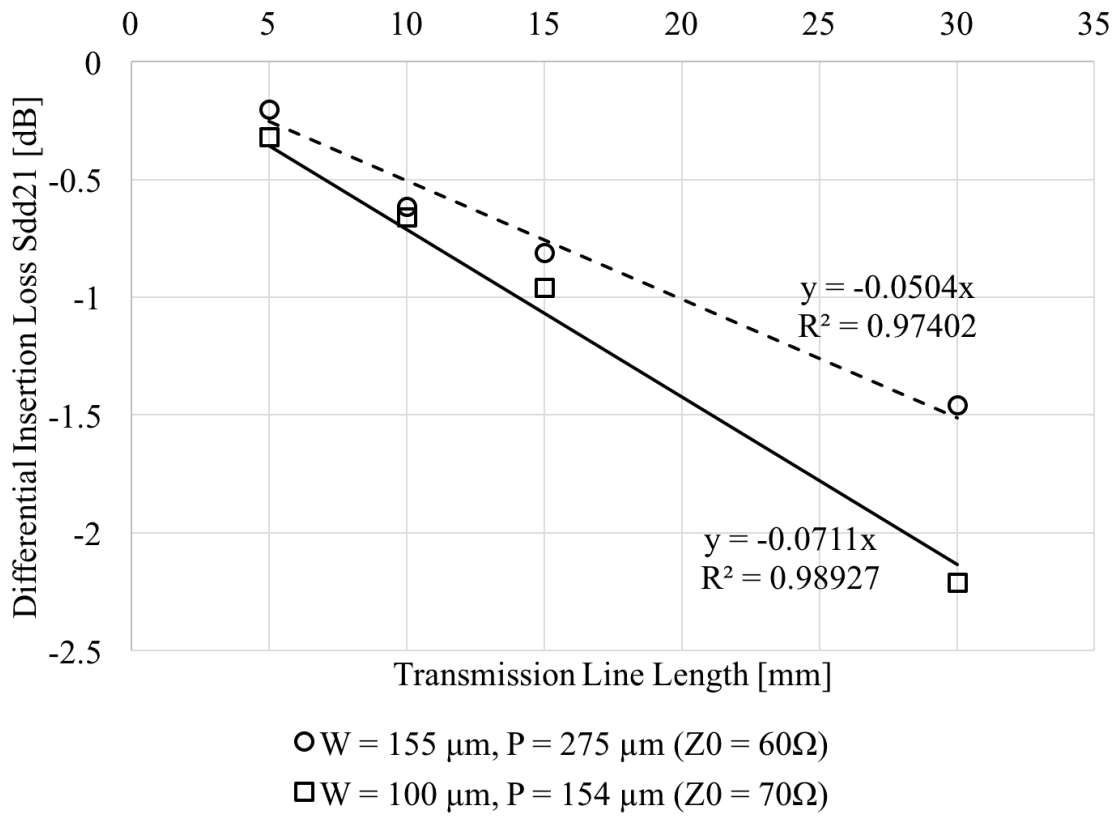


Figure 75. Normalized differential insertion loss of RDL on glass at 14 GHz.

and correlated well with simulation results in 4.1.1.

4.3.2 External I/O RDL Test Vehicle 2

Test vehicle 2 used the two-metal layer stack-up shown in Figure 77 with BCB polymer dielectric as a passivation layer where line pitch P = 150 µm at line width W = 100 µm to achieve Z_{diff} = 100 Ω. The primary focus of this test vehicle was the characterization of differential crosstalk without ground shielding, and the effect of TPV signal transitions on external I/O performance.

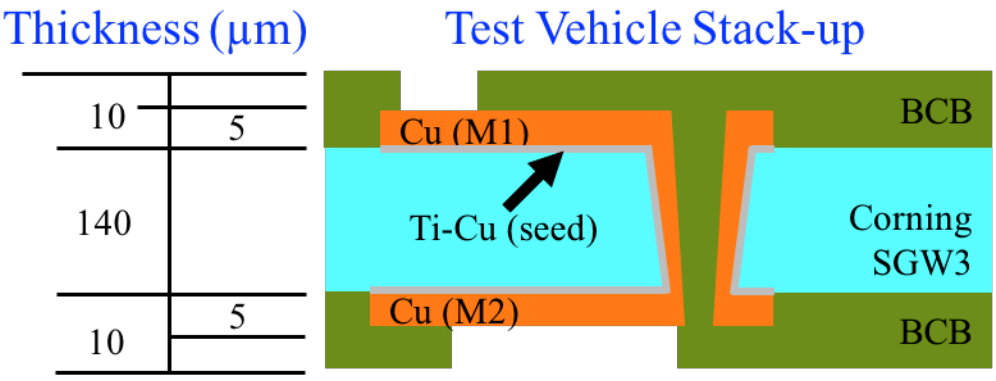
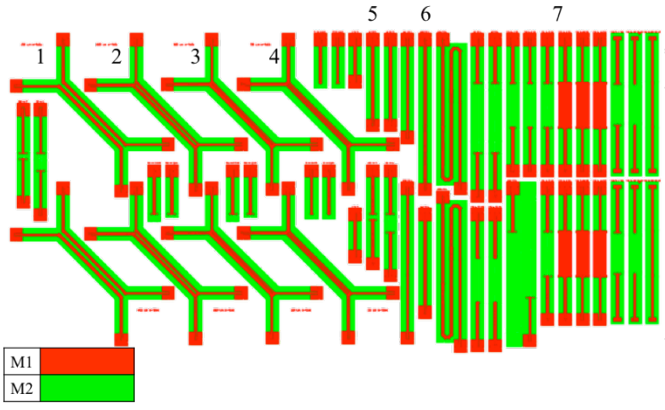


Figure 77. External I/O Test Vehicle 2 design rule.

This test vehicle was fabricated on 100 mm x 100 mm x 140 µm via-first glass panels provided by Corning Inc. with 75 µm TPV at 150 µm pitch to match the differential line pitch. Figure 76 shows the high frequency test structure layout on a two-metal layer glass panel. Due to ground layer proximity differential crosstalk was expected to be higher compared to implementations in build-up layers with thinner dielectric,



Test Structure	Specifications
1	Differential crosstalk (pS = 400 µm)
2	Differential crosstalk (pS = 200 µm)
3	Differential crosstalk (pS = 100 µm)
4	Differential crosstalk (pS = 50 µm)
5	10 mm line
6	17.3 mm line
7	15.3 mm line with TPV

Figure 76. External I/O Test Vehicle 2 two-metal layer layout.

which affords tighter ground coupling. Four crosstalk test structures were included in the design at differential pair spacing pS = 50 – 400 µm to determine the effect on pair spacing on crosstalk up to 40 GHz. The design also included on-panel calibration structures. Differential MSL thru structures used for de-embedding and TPV transition analyses are shown as test structures 5 – 7 in Figure 76.

Test vehicle 2 used the same process flow discussed in 4.3.1. Following the SAP, a 10 µm thick BCB PID film provided by Dow Chemical was applied using a vacuum lamination process. For this particular test vehicle, this dry film dielectric served as a passivation layer, but can be used as an interlayer dielectric between a high speed routing layer and high density routing layers for wide I/O. Glass panel fabrication was completed

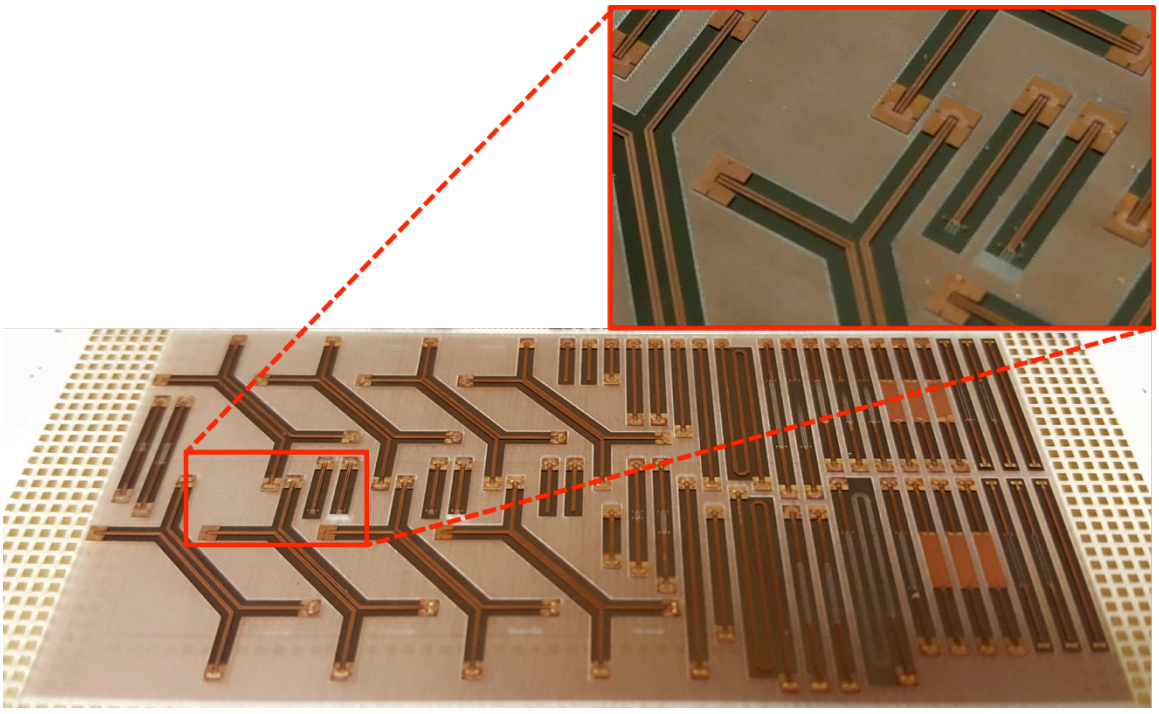


Figure 78. External I/O RDL Test Vehicle 2 panel fabrication results.

after applying an electroless nickel immersion gold (ENIG) surface finish. High requency tests, however, were performed prior to this surface finish, therefore they did not consider effects of this metallization on line performance. Top views of the fabricated glass panels with the high frequency test structures are shown in Figure 78.

4.3.2.1 Measured Differential Crosstalk

High frequency test structures were characterized courtesy of Ciena Corp. using a Rohde and Schwarz two-port 40 GHz Vector Network Anlayzer (VNA) and six-port switch matrix. The measurement setup is shown in Figure 79, which depicts the single-

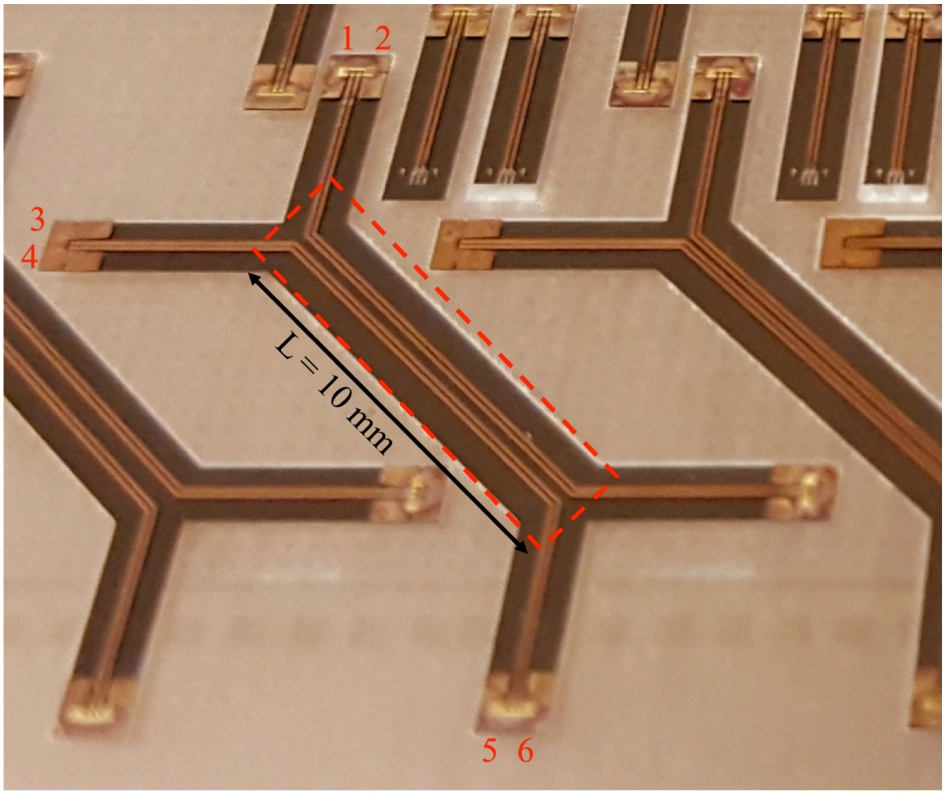


Figure 79. Crosstalk measurement setup (*pS* = 200 µm).

ended port assignment. The remaining ports were terminated with Z_0 = 50 Ω loads. After calibration, the reference plane was set at the probe tips.

Further de-embedding to remove pad effects was not performed for crosstalk structures due to the test structure geometry. Coupling coefficients between perpendicular differential lines, pads, and probes were negligible since the signal launch pads were orthogonal. Therefore, the resultant differential crosstalk was mainly determined by the area where pair spacing is less than 400 μm and differential pairs are parallel as highlighted in Figure 79.

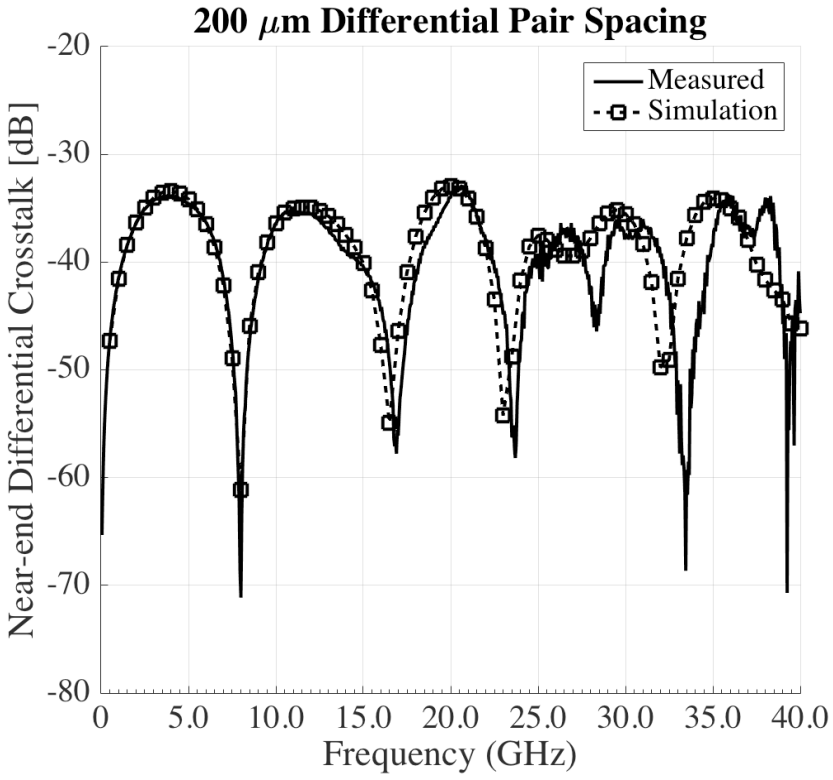


Figure 80. Near-end differential crosstalk without ground shielding (*pS* = 200 μm).

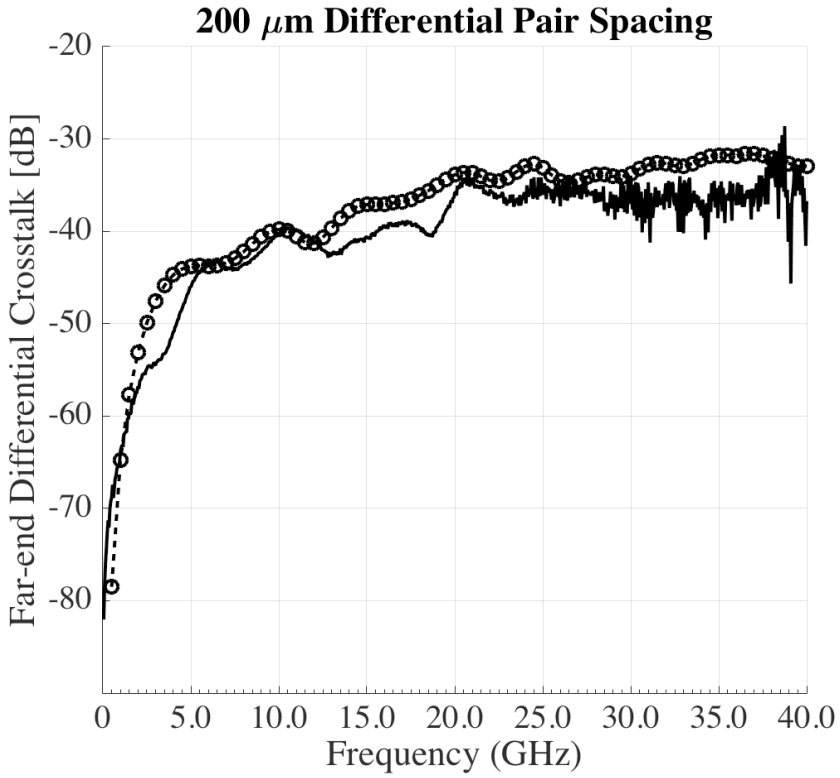


Figure 81. Far-end differential crosstalk without ground shielding (*pS* = 200 μm).

Model to hardware correlations for near- and far-end differential crosstalk at a pair spacing *pS* = 200 μm are shown in Figure 80 and Figure 81 respectively. In both plots, measured results are shown as a solid line and simulation results are shown as a dashed line with a marker. Excellent model to hardware correlation was observed up to 25 GHz with fair correlation up to f = 40 GHz. A shift in resonance points up to $\Delta f \approx 2$ GHz beyond 25 GHz was observed in near-end crosstalk compared to simulations. Deviations between the simulated and measured results are expected for far-end crosstalk measurements due to the low signal strength less than -35 dB. Most importantly, the results confirmed the maximum differential crosstalk across the measured frequency range, and was less than -30 dB for *pS* greater than 200 μm without ground shielding.

4.3.2.2 Effect of TPV on 28 Gbps External I/O

High frequency test structures 5 – 7 shown in Figure 76 were characterized courtesy of Ciena Corp. using a Rohde & Schwarz 4-port 67 GHz VNA measurement setup. After calibration, the reference plane was set at the probe tips. Split scattering parameters (S-parameter) were extracted for the 10 mm thru test structure 5 using auto fixture removal (AFR) available in Keysight™ Physical Layer Test System. These AFR-generated S-parameters were used to de-embed pad effects using a de-embed S-parameter data component in Keysight™ Advanced Design System shown graphically in Figure 82. The 17.3 mm thru test structure 6 was measured, and pad effects on the S-parameter measurement were de-embedded to yield the S-parameters for a L = 7.3 mm M1-MSL

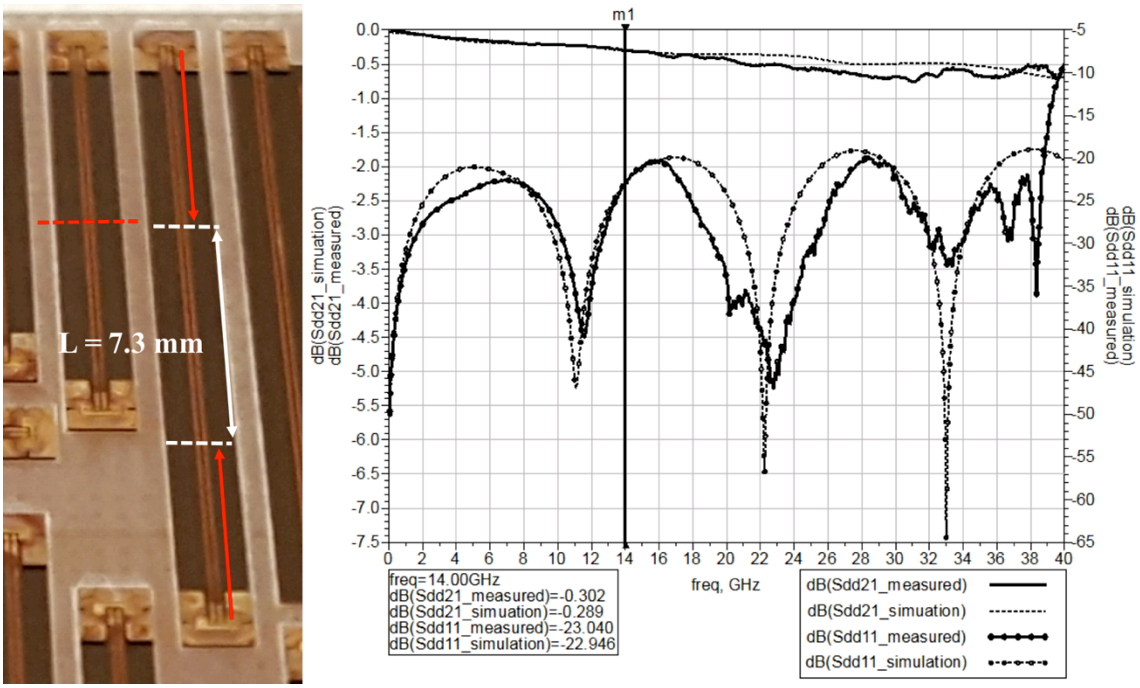


Figure 82. De-embedded S-parameter measurements using test structures 5 and 6.

differential pair with good model to hardware correlation up to 40 GHz. The same procedure was used to de-embed pad effects on test structure 7. After pad de-embedding, an MSL-to-MSL S-parameter with M1 MSL length L_{M1} = 0.1 mm and M2 MSL length L_{M2} = 5 mm with two TPV transitions was extracted.

The extracted S-parameter files were used to simulate the eye diagram for 28 Gbps non-return to zero (NRZ) external I/O signaling with and without TPV transitions. Time domain simulation included 28 Gbps transceiver behavioral models provided courtesy of

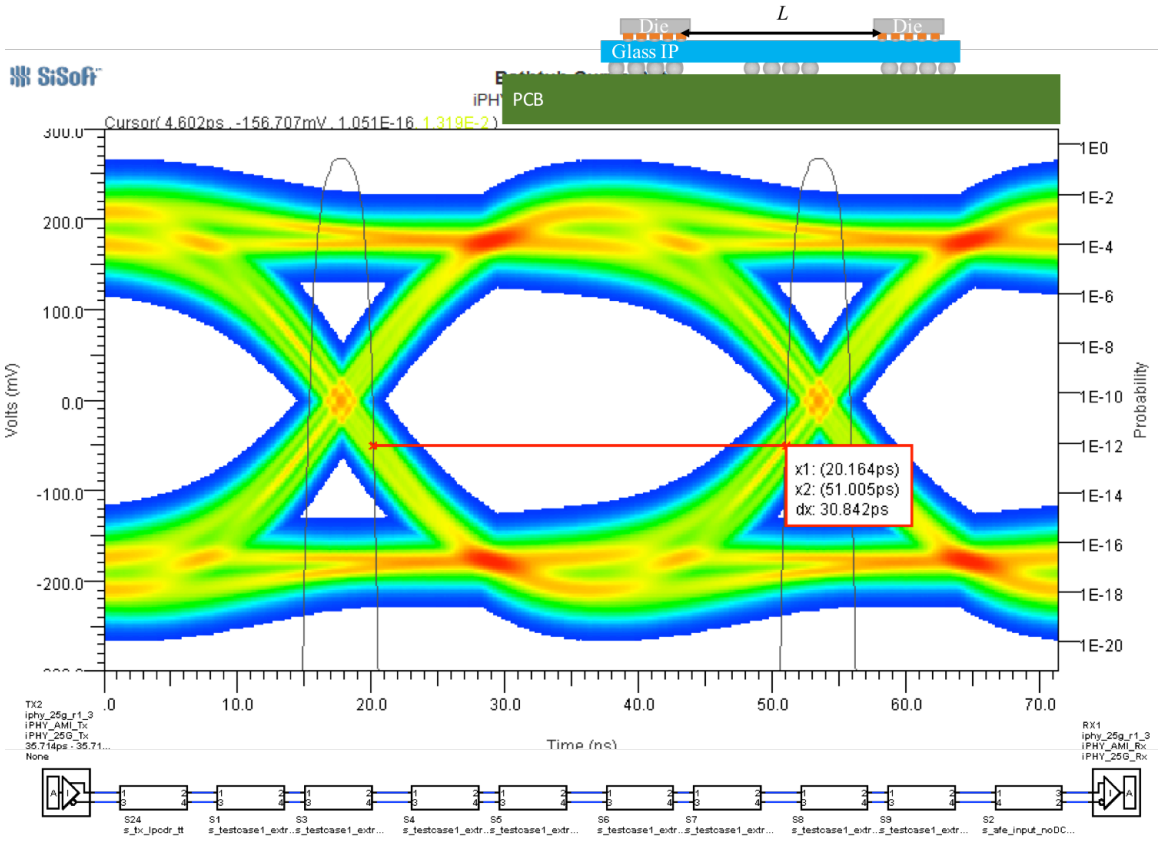


Figure 83. Test Case 1 simulated eye diagram at 28 Gbps NRZ (L ≈ 60 mm).

Ciena Corp. Two test cases were considered for eye diagram simulations:

1. Die-to-die on glass with no signal transition (M1-MSL) at L = 7.3 mm, 14.6 mm (2x), 29.3 mm (4x), and 58.4 mm (8x)
2. Die-to-die on glass with TPV transitions (MSL-to-MSL) with M1-MSL cascaded with MSL-to-MSL S-parameters to simulate L = 19.6 mm (with two TPV transitions)

Simulated eye diagrams for test cases 1 and 2 are shown in Figure 83 and Figure 84

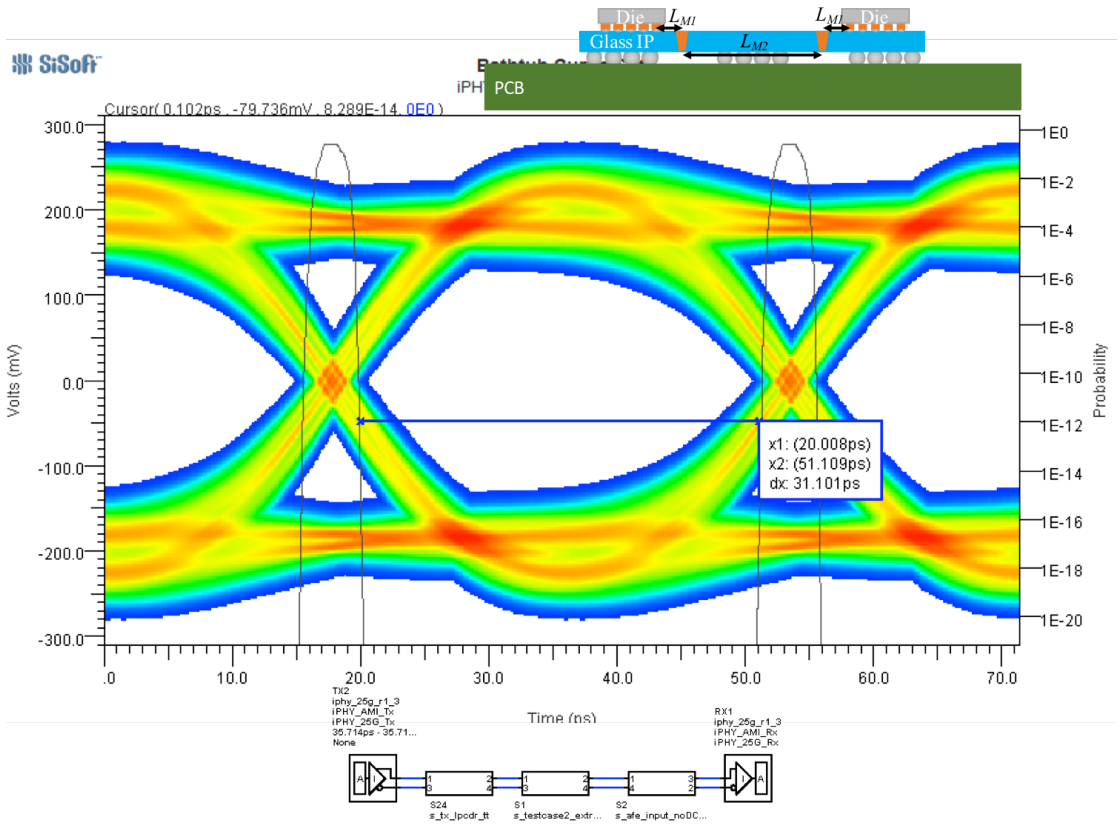


Figure 84. Test Case 2 simulated eye diagram with TPV at 28 Gbps NRZ (L ≈ 20 mm).

respectively. The eye diagram for test case 1 is for the 8x setup according to the simulation test bench shown in the cutout of Figure 83. Simulated eye performance did not include the effects of crosstalk and PDN induced jitter, and used IBIS models with equalization turned off for all test cases.

A large eye opening 0.86 UI at a bit error rate BER = $1x10^{-12}$ without digital feedback equalization (DFE) at $L \approx 60$ mm for test case 1 was observed, and was attributed to the low line attenuation exhibited by RDL on glass. Furthermore, the effect of TPV transitions was negligible on external I/O performance. An eye opening 0.86 UI at BER = $1x10^{-12}$ without DFE was observed for test case 2.

4.4 Summary

High speed channels for external I/O were implemented using RDL on glass to improve conductor and dielectric losses and address the technical challenges identified in Table 2. A major design challenge for wafer-based silicon interposer was line attenuation due to RDL coupling to the silicon substrate and TSV capacitive loading and crosstalk. The design and demonstration of RDL on glass for high speed external I/O verified line attenuation as low as -0.05 dB/mm at 14 GHz. Surface roughness R_a less than 5 nm, loss tangent $tan\delta = 0.005$ at 20 GHz, and large conductor cross section greater than 100 μm^2 improved line attenuation compared to silicon.

High frequency characterization and eye diagram simulation at 28 Gbps NRZ was used to verify low crosstalk and low loss at TPV transitions. Differential pair spacing greater than 200 μm was required to achieve less than -30 dB differential crosstalk up to 40 GHz. Line pitch and width equal to TPV (as well as CLI bump pitch) was used to

remove differential fan-out and improve differential insertion loss. Channel performance for 28 Gbps was compared with and without TPV transitions using measured S-parameters and high speed transceiver behavioral models. Time domain simulations showed 0.86 UI at BER = $1x10^{-12}$ without equalization. Most importantly, this high speed channel analysis showed that the glass TPV was electrically transparent at 14 GHz, and demonstrates the bandwidth scalability of a 2.5-D glass interposer package for die-to-board channels.

Therefore, high speed RDL on glass with fine pitch TPV shows great potential to scale data rates beyond 28 Gbps at lower signal power and higher bandwidth density compared to silicon interposers, which must consider interposer RDL, TSV, and added signal transitions between the die and PWB for external I/O performance.

CHAPTER 5. DESIGN AND DEMONSTRATION OF FULLY INTEGRATED 2.5-D GLASS INTERPOSER PACKAGES

The previous two chapters described the fundamental research in modeling, design, fabrication and characterization of low loss RDL and low latency RDL on glass interposers for external I/O and wide I/O respectively. This chapter describes the design and demonstration of a 2.5-D glass interposer test vehicle that integrated these RDL designs on 100 µm thick 150 mm x 150 mm glass panels with through vias. Figure 85 shows the targeted six-metal layer stack-up, and Table 7 provides a detailed design rule summary. Design rules in Table 7 are based on the results described in Chapter 3 and

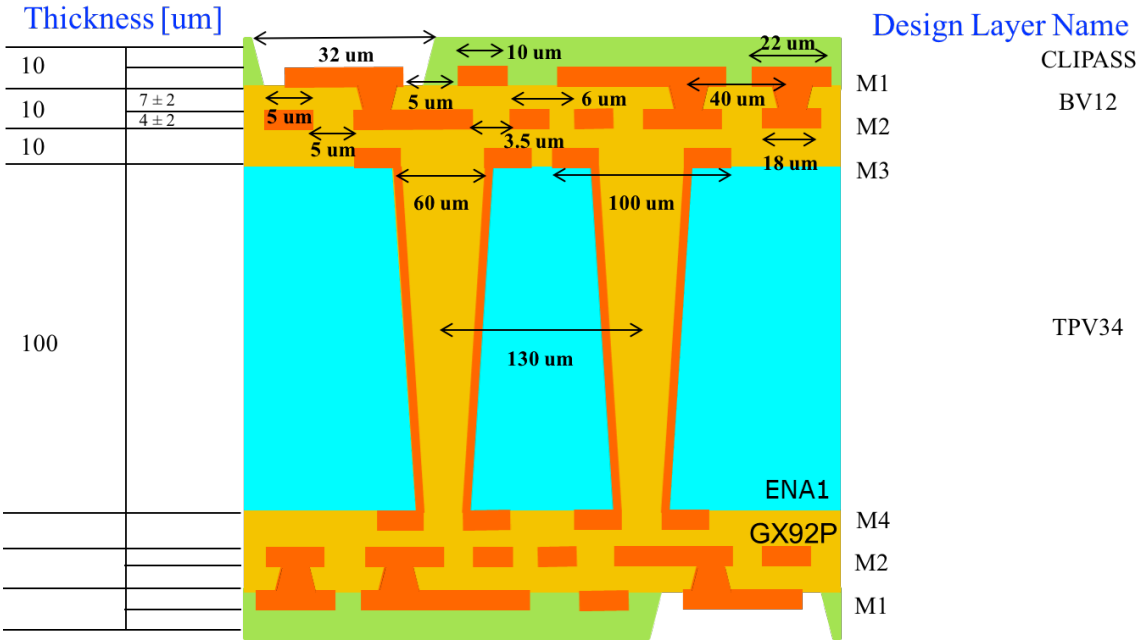


Figure 85. 2.5-D glass interposer test vehicle stack-up.

Table 7. Design and demonstration test vehicle design rule summary.

Design Layer	Description	Minimum Rule
M1	Line pitch/width	20/10 µm
	Pad-to-line space	5 µm
M2	Line pitch/width (die escape)	6/3 µm
	Pad-to-line space (die escape)	3.5 µm
	Line pitch/width	10/5 µm
	Pad-to-line space	5 µm
M3	Line pitch width	20/10 µm
	Pad-to-line space	5 µm
BV12	Top capture pad (M1)	22 µm
	Bottom land pad (M2)	18 µm
	Via diameter/pitch	8/40 µm
TPV34	Top capture pad (M3)	100 µm
	Bottom land pad (M4)	100 µm
	Via diameter/pitch	60/130 µm
CLIPASS	NSMD SRO	32 µm

Chapter 4 that meet the wide I/O and external I/O electrical design objectives outlined in Table 2 for a 2.5-D glass interposer package.

The 2.5-D glass interposer test vehicle was designed to demonstrate the integration of fine pitch multilayer RDL and thermo-compression bond (TCB) processes on a larger than reticle interposer to achieve wide I/O interconnection densities consistent with HPC system requirements. These processes were integrated with through vias in glass that were formed using via-first methods. Via-first referred to the state of the glass panels before RDL fabrication. Glass panels were received with predrilled TPV. The first

fabrication step, therefore, required metallization of TPV in thin glass, and then subsequent RDLs were formed using panel processes.

A symmetric dielectric and metal layer stack-up was used with TPVs to demonstrate the full integration of RDL with TPVs, although the TPVs in the first test vehicles were not electrically connected to the fine pitch routing layer M2. The targeted interposer body size was 38 mm x 30 mm x 0.160 mm (37% larger than 65 nm BEOL silicon wafer reticle). The total interposer thickness does not include C4 bumps and was based on 100 μm glass core and 10 μm dielectric build-up film thicknesses.

A single fine-line routing layer M2 was included in the design to demonstrate 100 lines/mm in a three metal layer stripline (ground-signal-ground) stack-up. The targeted copper thickness was based on modeling and simulation results for wide I/O in 3.1.2, which showed that interconnect cross section A = 12 μm^2 reduced interconnect delay by 25% to t_d = 0.015 UI/mm compared to BEOL RDL.

The top metal layer M1 was implemented as a routing layer using a non-soldermask defined (NSMD) solder resist opening (SRO). Routing on the top metal layer was beneficial in reducing layer count and interposer cost where typical 2.5-D implementations reserve the top metal layer for copper pillar bump landing pads, necessitating an extra RDL layer. Top layer routing density can be improved using a soldermask defined (SMD) SRO, but this design required further process optimization to improve the chip-level interconnect yield.

5.1 Panel Scalable Fabrication Process Flow

The redistribution layers in the 2.5-D glass interposer test vehicle were fabricated using double-sided and panel-scalable processes consistent with the packaging cost requirements for high performance systems outlined in 1.1. Test samples were fabricated on 100 – 300 μm thick 150 mm x 150 mm glass panels using a process flow that is scalable to 500 mm panel size to achieve high density RDLs at 40 μm bump pitch and below. Contributing factors to reducing the 2.5-D glass interposer package costs in addition to potential economies of scale of large panel fabrication included the use of high-throughput packaging processes, low cure temperature dry film polymers for build-up dielectrics, and high routing density to reduce layer count. The fabrication process flow for a fully-integrated, six-metal layer 2.5-D glass interposer package is summarized in Figure 86.

The demonstration of external I/O and wide I/O RDL discussed in previous chapters was on separate glass test vehicles and did not require the full process flow as noted in Figure 86. High speed RDL signal layers were reserved for copper traces directly on glass. Therefore, the first SAP used a sputtered Ti-Cu seed layer to increase copper trace to glass adhesion. A basic clean and plasma (O_2) descum was used prior to SAP1 metallization on glass. After seed layer deposition, a dry film photoresist (DFR) was roll laminated on each side of the via-first glass panel and patterned using projection lithography. Electrolytic plating was used to form the RDL after DFR exposure and development. The first SAP was completed after DFR strip and seed layer etching, which required a copper etch and titanium etch.

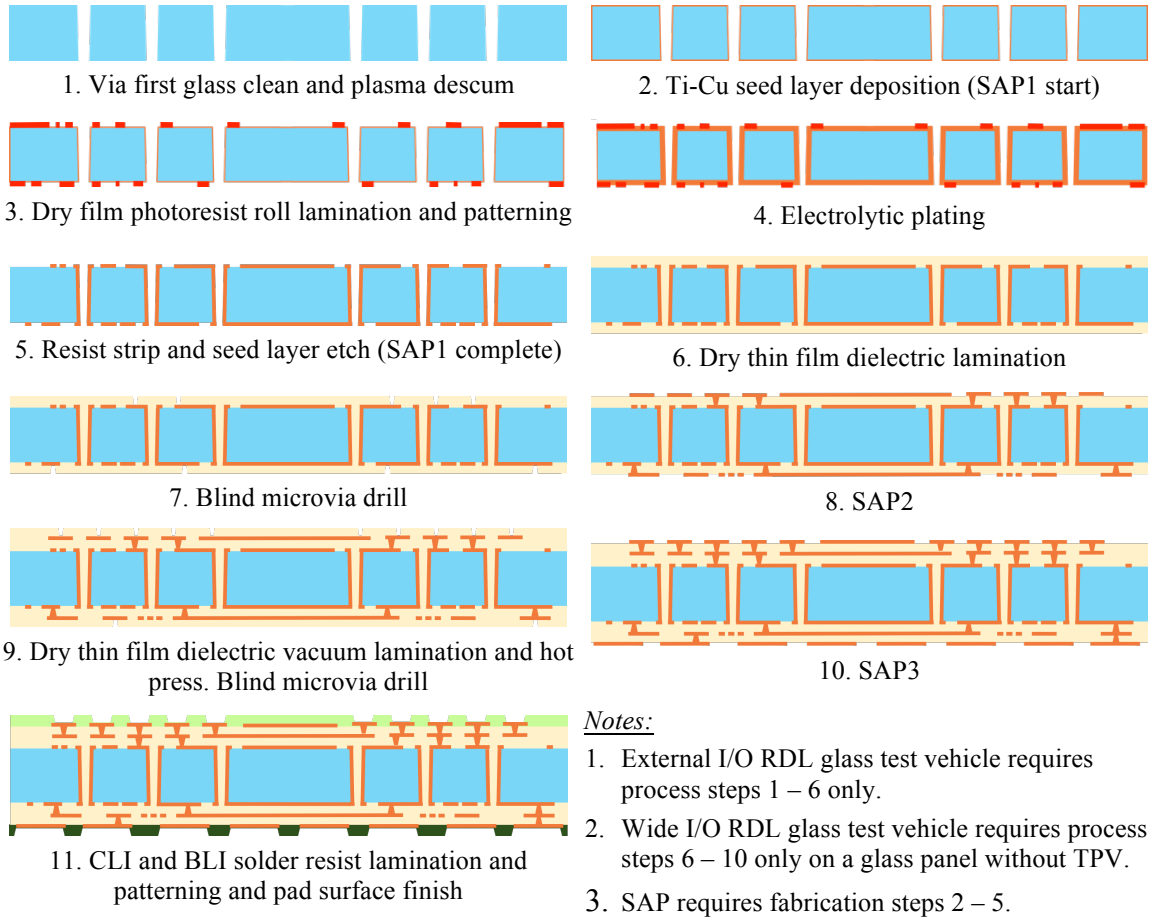


Figure 86. Fully integrated low cost panel-based glass interposer process flow.

Subsequent build-up layers used an electroless (e-less) copper seed layer for SAP and required copper seed layer etching only. A dry thin film dielectric was vacuum laminated on both sides of the glass panel after SAP1. Hot press was used before microvia drill to improve dielectric planarity required for fine line photolithography.

A second SAP was used to form high density RDL and fill the drilled microvias. Fabrication processes six through eight in Figure 86 can be used iteratively to form multiple high density RDL as required by the electrical design. A single fine pitch RDL routing layer was used, based on the ground-signal-ground layer assignment for wide I/O.

The glass interposer panel fabrication was completed after chip- and board-level interconnect passivation and surface finish.

5.2 Electrical Designs for Test

Multiple designs for test (DFT) were implemented during glass interposer fabrication to identify the yield limiting process steps. Test structures to determine individual process yields for TPV metallization, fine line SAP, blind microvia laser ablation and metallization, and fine pitch two-metal layer RDL were included in each coupon and panel where each panel included eight test coupons. Design for test considerations were also included in the bump and pad design for chip-level assembly. This included multilayer die-to-die routing structures, as well as isolated chip-level assembly test structures. The following sub-section provides the design details for each test structure. In general, coupon and panel design included direct current, open-short electrical test structures only. High frequency RDL tests were included in the RDL test vehicles discussed previously.

The interior metal layers, M3 and M4 in Figure 85, were connected using 60 μm TPVs at 130 μm pitch. These routing layers were not electrically connected with the subsequent layers. Therefore, exterior metal layers, M1 and M2, were fabricated on both sides of the glass panel after TPV metallization. Through package via metallization quality and yield was tested using daisy chain test structures as shown in Figure 87, with various numbers of TPV included in the interconnect path. Test structures used a 16 x 16 TPV array placed below die corners and fine pitch RDL routing areas fabricated in subsequent processes. This placement of TPV arrays was intended to study the effect of

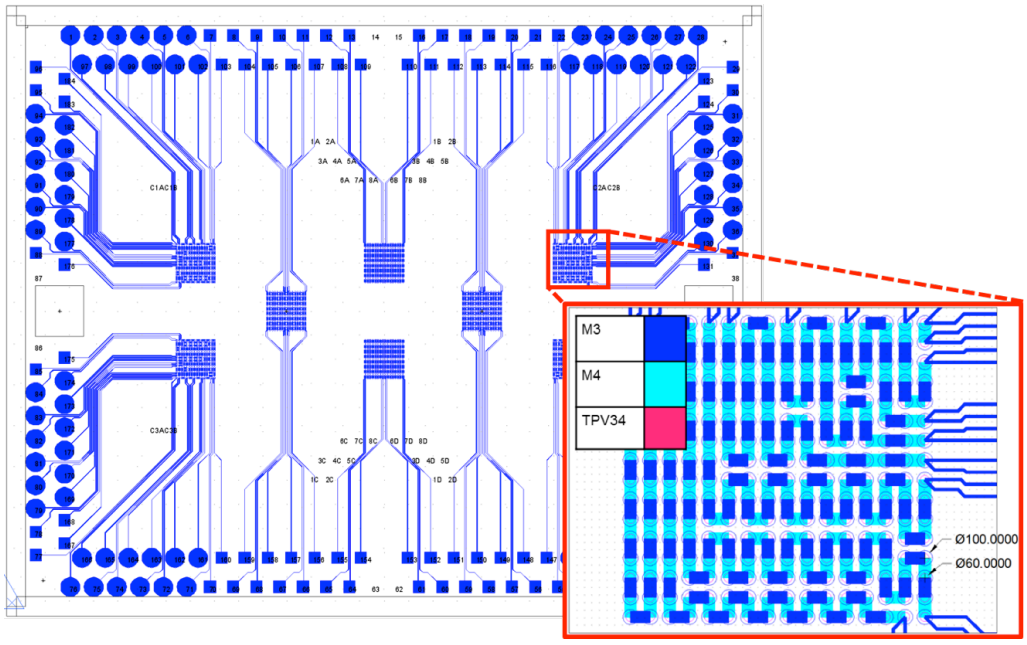


Figure 87. TPV array daisy chain test structures.

TPV structures on surface planarity and lithography. Forty-five, four-point probe reliability test structures were included in each coupon containing a minimum of two TPVs and a maximum of up to 128 TPVs per test structure. Variations containing two, 64, 66, and 128 TPVs were selected for process screening, while the remaining test structures were used for failure analysis.

Fine line test structures shown in Figure 88 were a unique interdigitated structure mimicking die-to-die interconnect fan-out at 6 µm line pitch. Open-short testing and optical inspection was used to determine the process yield for die escape and fan-out lines. Variations of this test structure were included with different number of die rows escaped, ranging from one die row up to six die rows. Four lines could be escape routed per row at 40 µm CLI bump pitch, given the die escape design rules for M2, and a

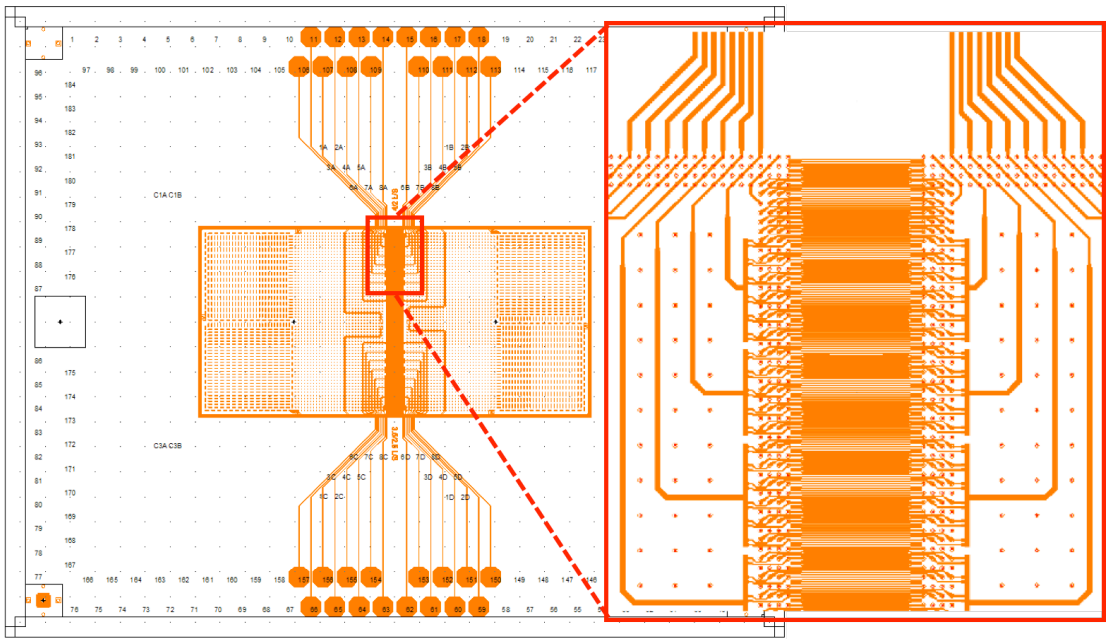


Figure 88. Fine pitch RDL open-short comb test structures.

maximum of 24 die-to-die interconnects (in six rows) were assessed in a single test structure.

Test points to analyze the process yield for microvia ablation at 40 µm via pitch are shown in Figure 89. Two-point probe measurements were performed on blind microvias near the die corners after completing M1 fabrication by SAP to determine the yield of interconnections between the top routing layer and fine line M2 routing layer.

Fine pitch, two-metal layer SAP RDL test structures are shown in Figure 90. These test structures were considered fully integrated 2.5-D routing structures that assess the integration yield of fine pitch CLI, blind microvia, and fine line SAP processes to implement low latency wide I/O interconnects.

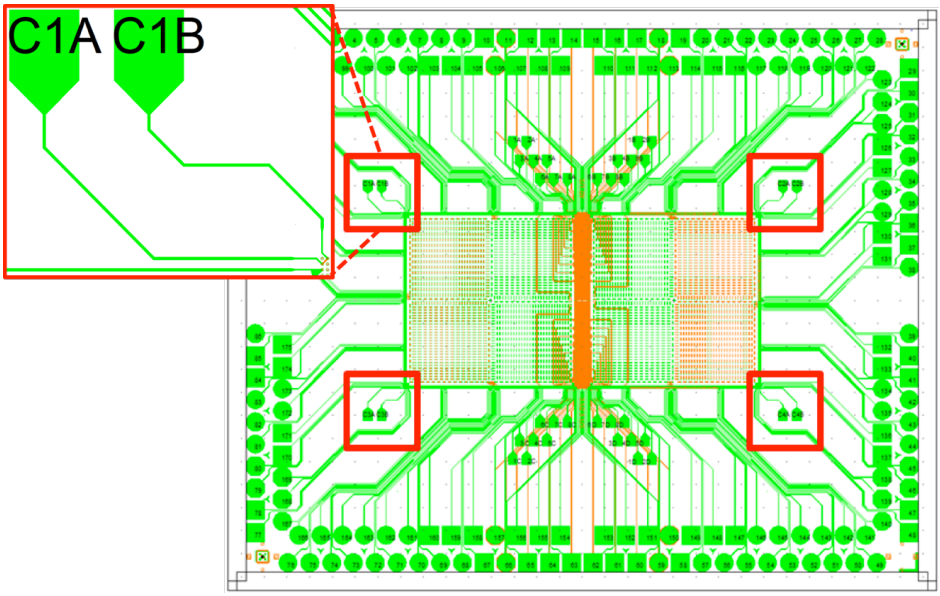


Figure 89. Blind microvia two-point test structures.

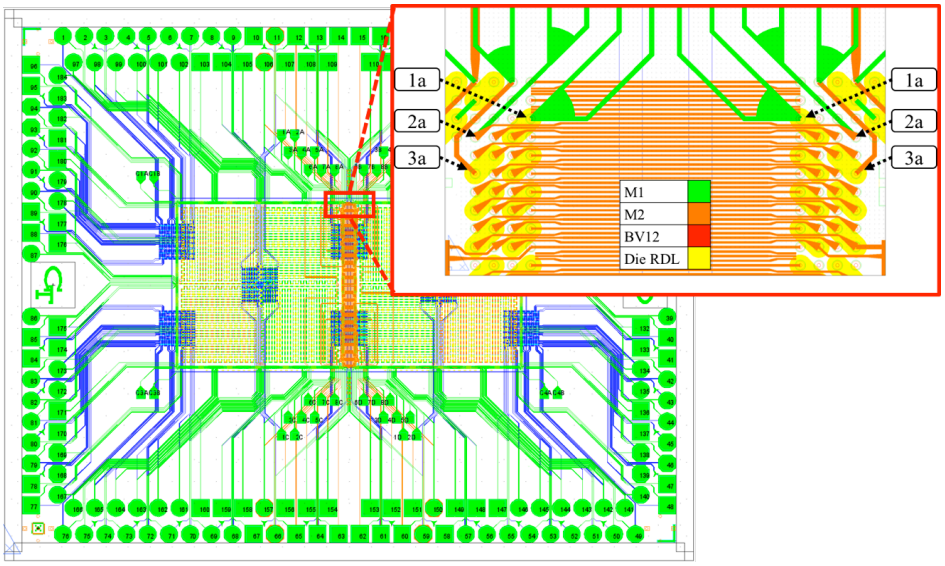


Figure 90. Fine pitch multi-layer RDL and chip level assembly test structures.

Two variations on these fully integrated test structures were included to isolate the effect of chip-level assembly process yield. Four-point probe tests at 1a-1b as well as 3a-3b were used to determine the yield of fine pitch RDL and assembly. Test points 2a-2b

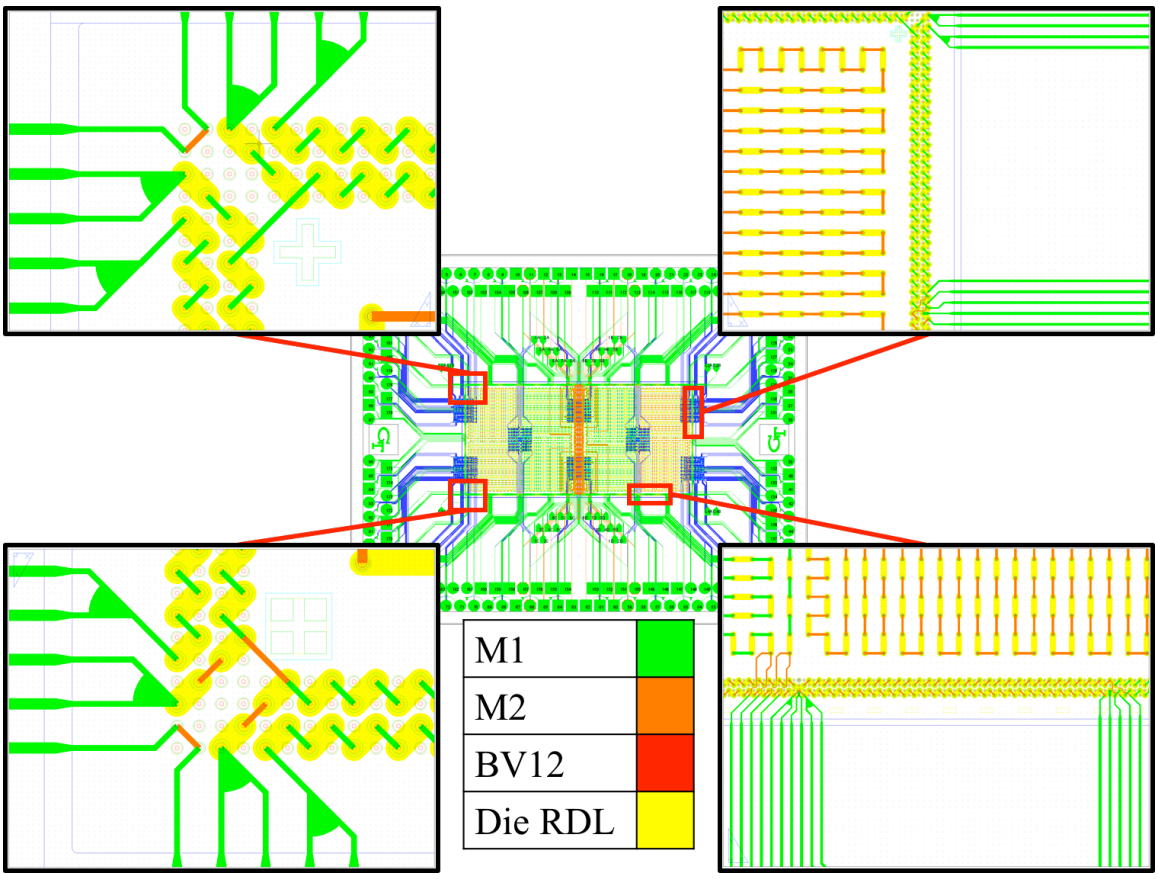


Figure 91. Chip-level assembly test structures at 56 µm bump pitch.

bypassed assembly yield to analyze the integration of fine line SAP with fine pitch microvias.

The coupon design included chip-level assembly test structures as shown in Figure 91 that were decoupled from fine line SAP processes to critically examine 2.5-D TCB process yield. Assembly test structures were implemented with coarse RDL routing at 20 µm line pitch and 10 µm line width to minimize RDL yield loss. Design variations at 56 µm bump pitch included test structures at the die corners with M1-Die routing (top left Figure 91) and M1-M2-Die routing (bottom left Figure 91) with eight die bumps per

structure. Test structures located on exterior bump rows were also included with M1-Die routing (top right Figure 91) and M1-M2-Die routing (bottom right Figure 91). Exterior bump test structure interconnect length varied and included up to 128 die bumps.

5.3 Glass Panel Fabrication

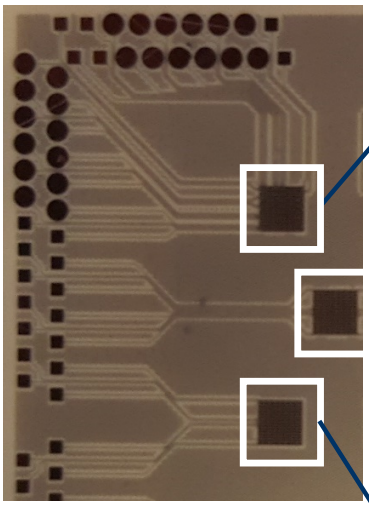
This section discusses the metallization of via-first TPVs in thin glass, the fabrication of fine line SAP RDL on glass with through vias, and the ablation and metallization of fine pitch microvias. The process yields of these fine pitch, multilayer RDL processes are analyzed based on the test structures described in 5.2.

5.3.1 Thin Glass Handling and Via-First TPV Metallization

Panels with TPVs fabricated in bare glass were provided by Asahi Glass Company (AGC), Japan [53]. A primer process was used to metallize the TPVs and improve 100 µm thick glass panel handling during the six-metal layer interposer fabrication [54]. The primer process created a 5 µm thin polymer buffer layer on the top and bottom surfaces

Table 8. Through package via reveal processes for via-first glass.

TPV Reveal Process	Yield
Maskless CO_2 laser drill	Poor laser alignment and excess polymer removal
Hard mask plasma reveal	Thin glass handling
Maskless plasma reveal	Excess polymer removal
Maskless UV laser drill	Accurate laser alignment and precise laser drill



Test Structure	Pass	Yield
TPV-NA-CL-002*	19	0.95
TPV-NA-CL-102*	20	1.00
TPV-NA-CL-202*	20	1.00
TPV-NA-CL-302*	20	1.00
TPV-NA-CL-066*	19	0.95
TPV-NA-CL-166*	18	0.90
TPV-NA-CL-266*	18	0.90
TPV-NA-CL-366*	19	0.95
TPV-NA-CL-064*	20	1.00
TPV-NA-CL-164*	17	0.85
TPV-NA-CL-264*	18	0.90
TPV-NA-CL-364*	18	0.90
TPV-NA-CL-464*	18	0.90
TPV-NA-CL-564*	19	0.95
TPV-NA-CL-664*	19	0.95
TPV-NA-CL-764*	19	0.95
TPV-NA-CL-0128^	19	0.95
TPV-NA-CL-1128^	18	0.90
TPV-NA-CL-2128^	16	0.80
TPV-NA-CL-3128^	20	1.00

*Number of TPV – last two digits

^Number of TPV – last three digits

Figure 92. TPV metallization yield in thin via-first glass using UV laser reveal.

of the glass panel, and required additional fabrication steps before the copper trace patterning by SAP1. Prior to seed layer deposition, a polymer dry film dielectric, with a nominal thickness of 5 µm, was vacuum laminated at optimized temperature and vacuum dwell time to achieve polymer tenting over the TPVs. Then, the TPV was revealed by removing the polymer on top and bottom surfaces around the TPVs, using one of four processes summarized in Table 8.

As seen in Table 8, TPV reveal included mask-based and maskless processes. The mask in this case referred to a hard copper mask, which required additional plating steps and often led to glass cracking during the handling of thin glass. Maskless processes used plasma and laser TPV reveal steps. Plasma and CO_2 laser TPV reveal processes resulted in excess polymer removal and subsequent copper delamination. A high precision ultra-violet laser was used to avoid damage to the surface polymer layer near the TPVs, and this front-up process resulted in improved TPV metallization yield as summarized for 20 test coupons in Figure 92.

5.3.2 Fine line SAP

Fine line RDL fabrication results on a 150 mm x 150 mm panel using an e-less SAP are shown in Figure 93. A line width compensation of +0.5 – 1.0 µm was used in the

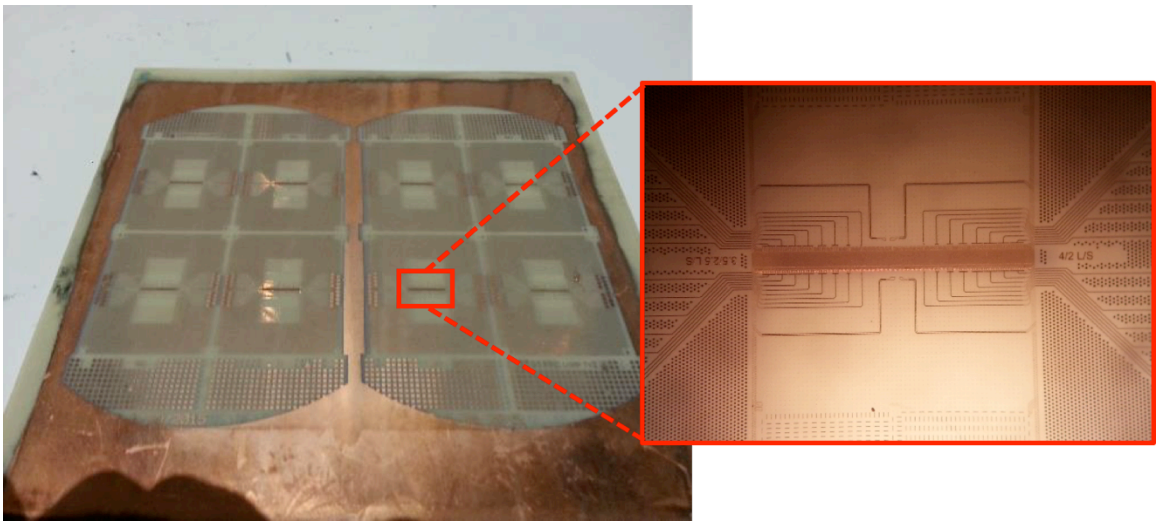


Figure 93. 6 µm pitch RDL fabrication on 100 µm thick 150 mm x 150 mm glass panel.

mask layout to achieve the design target line width after seed layer etch. Therefore, two layout variations to realize a 6 µm pitch RDL at 3 µm line were used, including 4 µm line at 2 µm space and 3.5 µm line at 2.5 µm space. Such mask compensation increased the risk of resist collapse and/or delamination after development, due to the reduced line to line gap (and hence the resist wall width). Optical inspection after resist development and plasma descum was used to confirm that there was no collapse or delamination in the photoresist layer.

After electrolytic copper plating to form RDL traces, processing challenges existed when stripping the resist layer. This was due to the high 1.33 aspect ratio of the fine pitch traces enabled by SAP. Fine pitch RDL after resist stripping is shown in the left micrograph of Figure 94 with no indication of resist residues. The final step in SAP was the copper seed layer etching to isolate the fine pitch traces. Differential spray copper

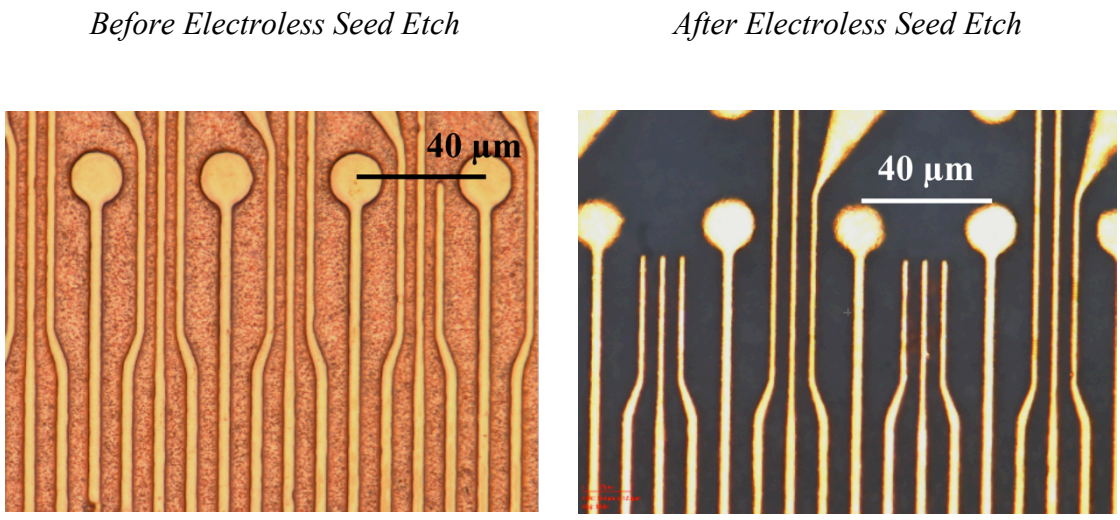


Figure 94. Fine pitch RDL SAP fabrication with electroless seed layer.

etching in addition to mask compensation was used to maintain 3 μm line widths [49]. Optical inspection of fine line structures, shown in the right micrograph of Figure 94, indicated 0.2 μm line narrowing as a result of side etching of the plated copper traces during seed layer etching.

Fine line SAP yield data is shown in Figure 95. The test structure name specified the number of lines included in the interdigitated test structure (e.g. '02' specified that eight lines are included). Yield data showed that seed layer etching was a critical fabrication step. With increasing line density, fine line yield showed a distinctive roll off from 0.90 to 0.60 when the number of interconnects increased from 12 to 16 traces in the

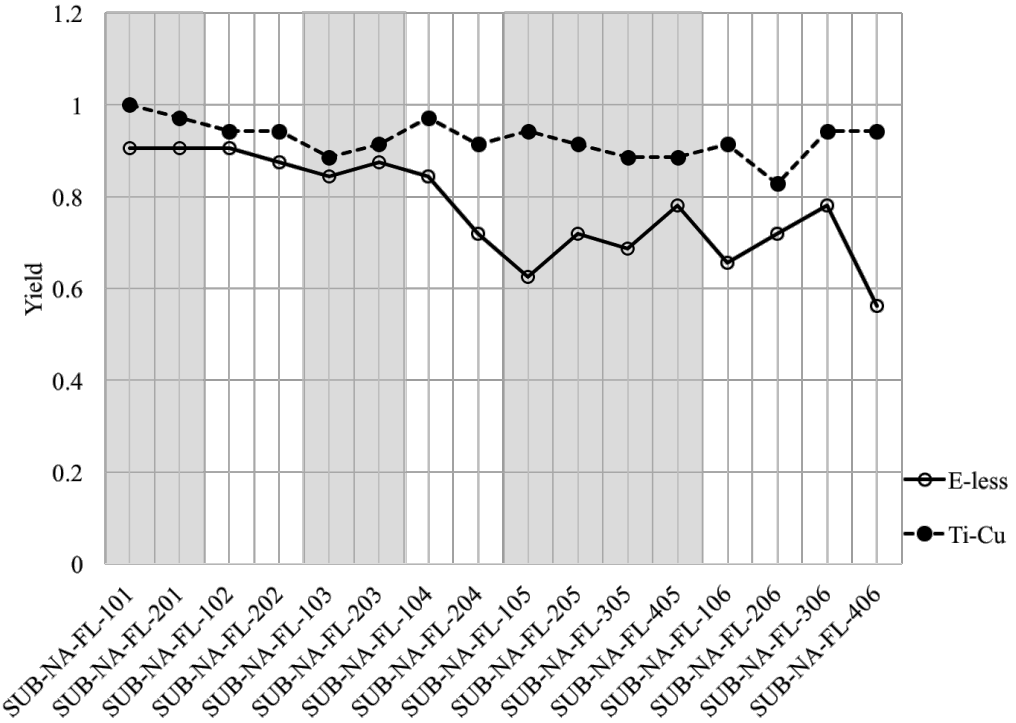


Figure 95. Fine pitch SAP yield with e-less copper vs Ti-Cu seed layer

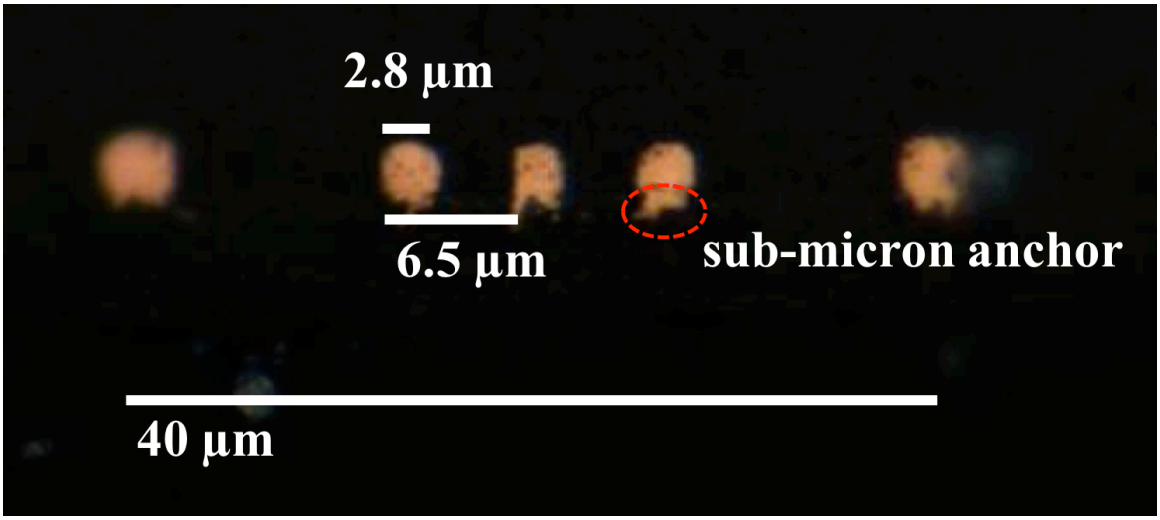


Figure 96. Electroless SAP 6 µm pitch RDL cross section.

test structure. Under etching was determined to be the root cause of failure upon panel inspection, which showed residual copper seed layer in high density routing areas, causing line shorting.

This residual seed layer was due to copper anchors extending down into the polymer dielectric sub-surface during electroless copper plating. Detailed analysis of cross section micrographs revealed sub-micrometer sized anchors in the seed layer as shown in Figure 96. These anchors were a result of the desmear step used to improve the adhesion between copper and the polymer as a part of the palladium catalyzed electroless copper deposition process. The desmear treatment was shown to increase the polymer surface roughness by up to R_z = 1.0 µm. Therefore, to remove anchors in the seed layer and achieve complete seed layer removal with good trace isolation, the etching time had to be extended, resulting in over etching of the traces. When the etching time was reduced, inadequate seed layer removal resulted in fine line shorting.

Fine line yield was improved by modifying the SAP with a Ti-Cu seed layer deposited using physical vapor deposition (PVD) instead of e-less copper plating. The Ti-Cu seed layer PVD process resulted in 30 nm titanium and 200 nm copper seed layer thicknesses. This required a two-step seed layer etch to remove copper and titanium after

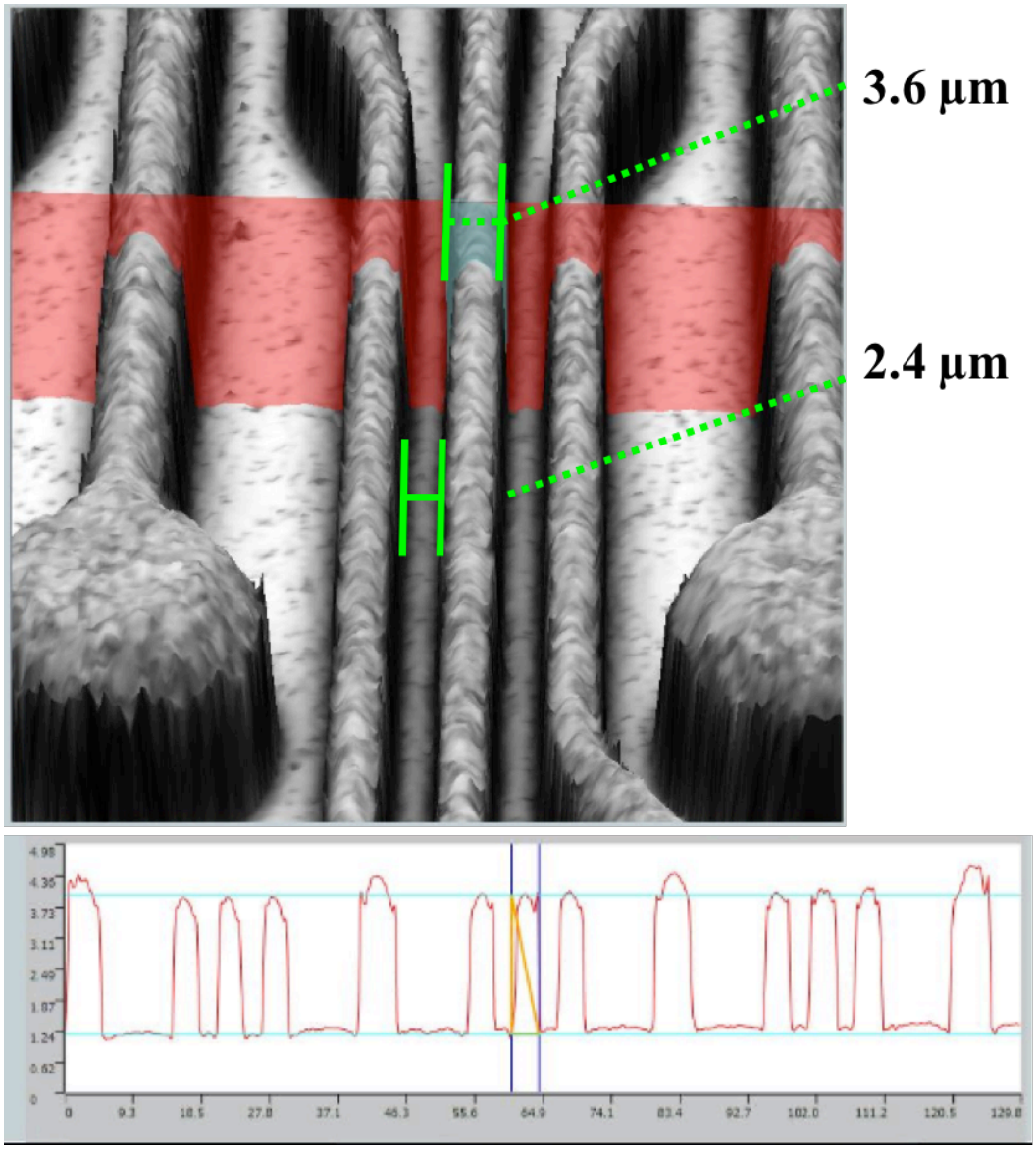


Figure 97. Fine pitch RDL SAP fabrication with Ti-Cu seed layer.

electrolytic plating. Differential copper spray etch was used to improve copper line profile as shown in Figure 97. Titanium acted as an adhesion layer to the polymer ILD mitigating the need for desmear roughening. Filler materials were not removed from the underlying ILD as a result and low surface roughness necessary for fine line yield was maintained. A Ti-Cu SAP resulted in higher yield compared to an e-less SAP as shown in Figure 95.

5.3.3 Micro-via ablation and metallization

Microvia ablation used a XeCl excimer laser (λ = 308 nm) scanning projection ablation process. A scan ablation technique was employed instead of a point-to-point laser ablation to increase process throughput when scaling to large panel processing. The scan ablation method utilized a quartz mask with sputtered aluminum openings to simultaneously ablate microvias over the entire 38 mm × 30 mm coupon area, which included a total of 14,704 vias (7,520 at 40 μm in line pitch and 7,184 at 150 μm in line pitch). Optical inspection and profilometry data were used to confirm that the vias were open and that the via side-wall angle was greater than 80°.

Minimizing the microvia capture pad size in order to increase interconnect density was critical to wide I/O line density as discussed in 3.1.3. Figure 98 shows the overlay accuracy of the scan ablation process across a 150 mm x 150 mm panel, enabled primarily by the dimensional stability of glass. The alignment process marker in the cutout of Figure 98 represents five capture pad diameters ranging from 18 μm down to 10 μm. This process marker was included in the corner of each coupon and was used to

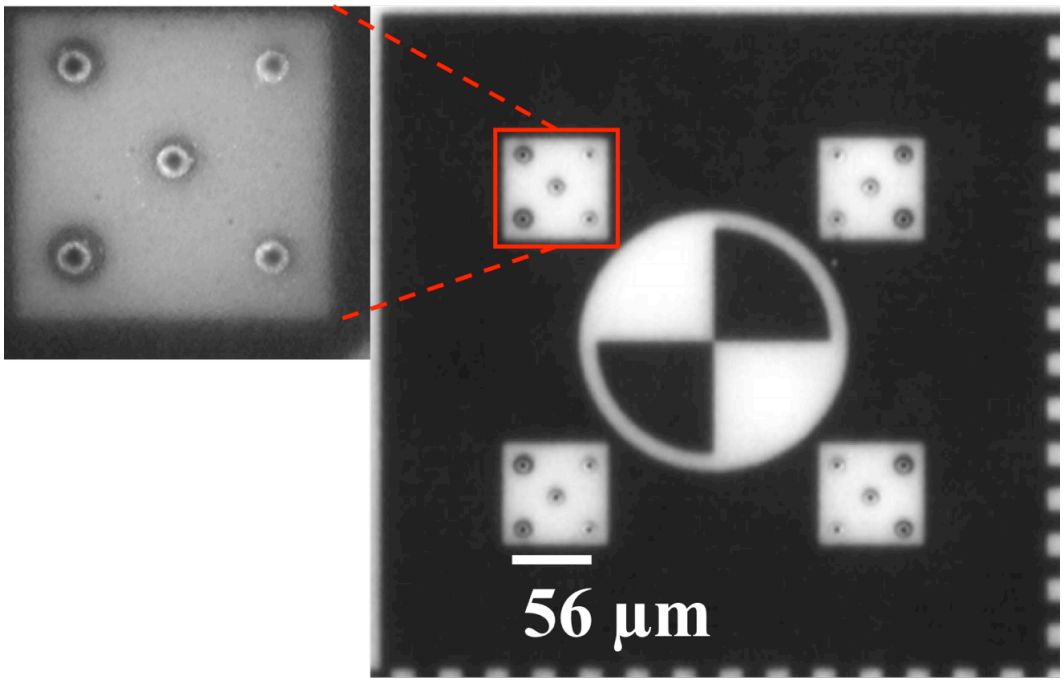


Figure 98. Blind microvia glass panel-level alignment at 40 µm pitch.

confirm less than 2 µm overlay accuracy across the panel, without alignment compensation during via ablation.

Achieving a fully-filled microvia without significant dimpling or dishing was considered critical for via-in-pad assembly yield when plating the top M1 routing layer. Furthermore, fully filled via plating will be required when scaling the fine pitch RDL processes to multiple fine line layers using stacked microvias. Figure 99 shows optical profilometry data obtained after M1 plating. The left micrograph in Figure 99 shows two capture pads included in one of the microvia test structures discussed in 5.2. The right micrograph in Figure 99 shows the two respective pad profiles indicating sub-micrometer

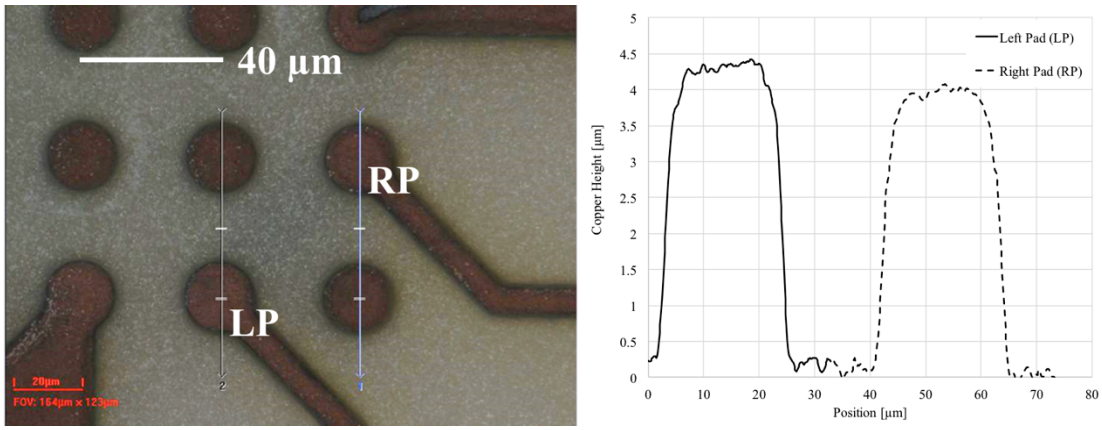


Figure 99. Blind microvia-in-pad plating.

topography at the top of the pad. Therefore, the plating conditions were sufficient to form flat pads for via-in-pad assembly.

Microvia yield was determined using the test structures shown in Figure 89 on 32 test coupons. A pass criterion of $R < 5\ \Omega$ was used since the two-point probe test caused increased resistance due to parasitic trace and contact resistance. An average panel yield of 0.88 was observed based on this test condition.

5.4 2.5-D Chip-level Assembly

A sequential pick-and-place TCB process, and a post-applied capillary underfill was used for 2.5-D chip-level assembly at 56 µm bump pitch and 100 µm die spacing. The assembled die was 10 mm × 10 mm × 0.2 mm with a four-row 80/40 µm staggered pin-out at the die periphery and a 150 µm full array interior pin-out (5456 total bumps). On-chip copper routing patterns were intended for electrical daisy chain connectivity tests only. The copper pillar with lead-free solder cap stack-up was 17/3/16 µm

Cu/Ni/SnAg at a 28 μm bump diameter. The following sub-sections describe the 2.5-D panel-level assembly process and results on 100 and 300 μm thick glass panels.

5.4.1 Panel-level Assembly Process

After completing glass interposer panel fabrication, bonding areas were treated using an acetone and isopropyl alcohol clean, and a prebake was applied. A no-clean flux was applied at the bonding site directly prior to die assembly, and the panel was placed on the assembly stage, which was kept at T = 70 °C in stand-by. Chip-level assembly was then carried out according to the process flow summarized in Figure 100. The first die was picked and placed using a 10 mm × 10 mm flat tool head, and the stage temperature was increased to T = 120°C directly prior to and during bonding. Thermo-compression bonding of the first die was carried out where the tool head temperature was ramped at 6 K/s to T = 390 °C. After a t = 3 s nominal dwell time, the tool head was cooled to T = 70 °C at 6 K/s. The bonding force was optimized using shear tests and cross section analysis. A constant bond force of F = 3 N was applied throughout the heating profile. The second die was assembled using similar TCB process conditions at a 100 μm die-to-die gap. This is a nominal die gap distance since die alignment and electrical die-to-die interconnect length is ultimately determined using complementary fiducials on the panel coupon and die.

Die assembly was checked prior to underfill dispense using test structures routed using M1 and die RDL only. After TCB was confirmed by open-short testing, bonding areas were treated using an acetone and isopropyl alcohol clean. The assembled panel

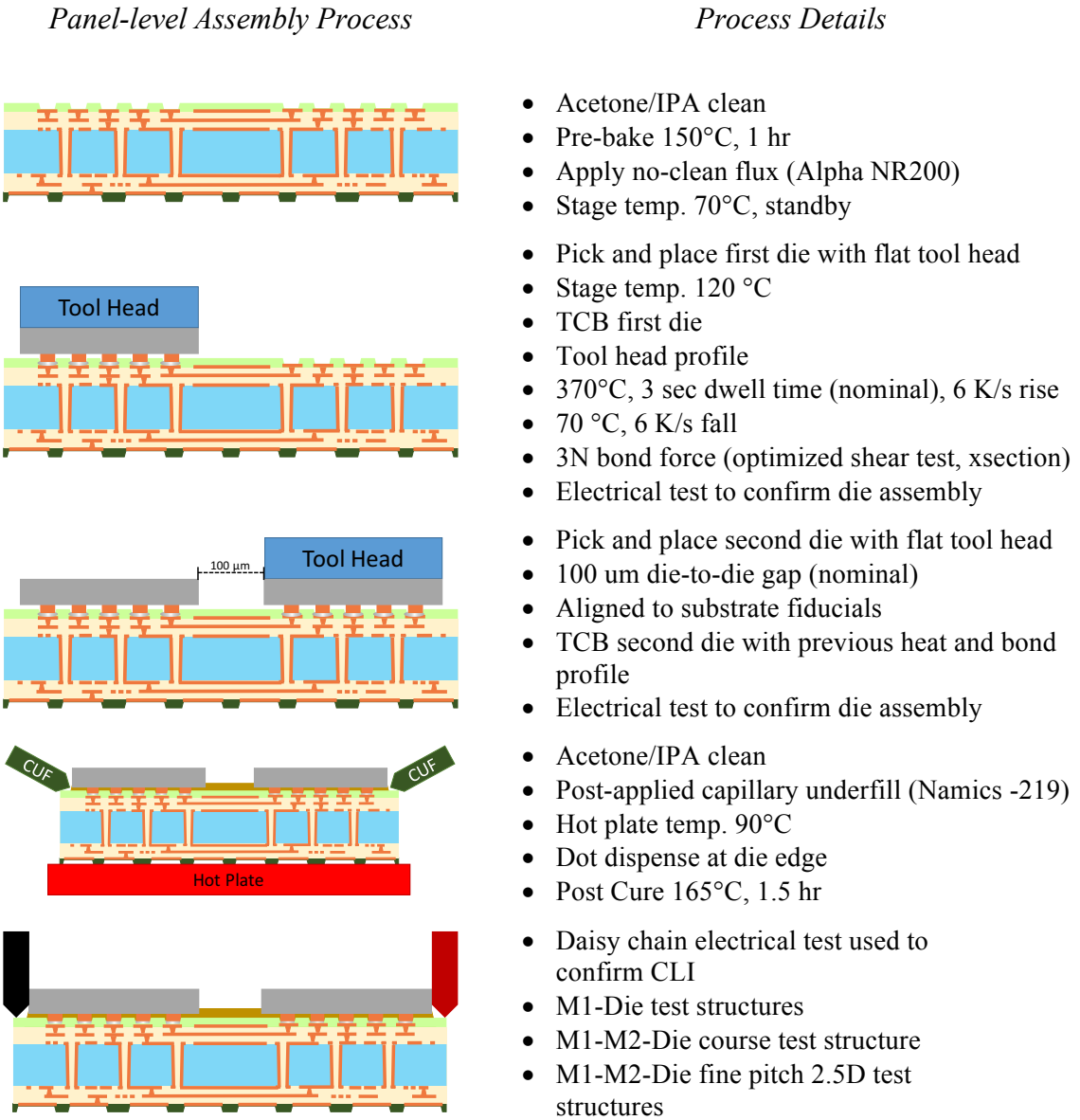


Figure 100. Panel-level fine pitch chip-level assembly process flow.

was then placed on a hot plate at T = 90 °C prior to underfill dispense. Underfill dispense volume was optimized to prevent overburden in the die gap. Also, to mitigate the risk of underfill voiding, a dual-point dispense technique was used where a dot underfill

dispense was applied at opposing die edges. Die assembly was completed after a post-dispense cure at T = 165°C for t = 1.5 hr.

5.4.2 Die Assembly and Characterization

Panel level 2.5-D assembly shown in Figure 101 was demonstrated on 300 µm thick glass interposers without TPV and 100 µm thick glass interposers with TPV as shown in Figure 102 and Figure 103 respectively. The detailed micrograph in the cutout of Figure 103 is looking from the coupon edge toward the 2.5-D die gap, and the detailed micrograph in the cutout of Figure 102 is viewing inward from the die gap toward the high density routing layer. Optical inspection of the 2.5-D die gap indicated that the post-applied capillary underfill flowed into the gap without overburden. Furthermore, the

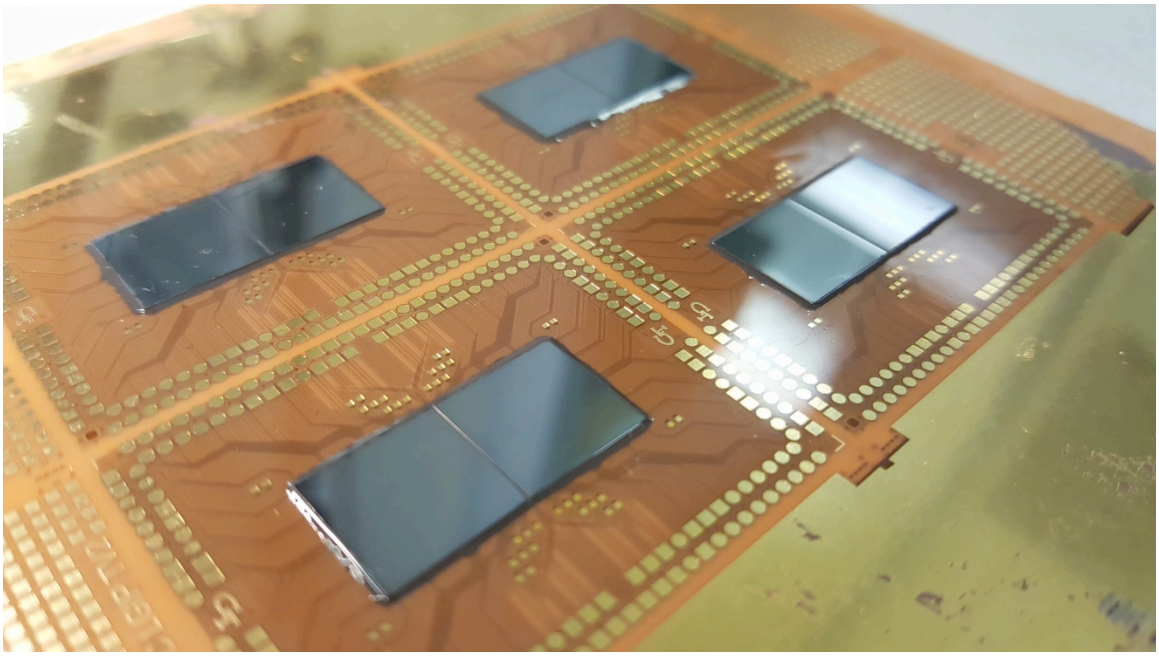


Figure 101. Panel level chip-level assembly on 100 µm thick glass panel.

detailed micrographs of the fine pitch solder joints indicated that a good chip-level interconnect was formed with minor solder depletion. Solder depletion was due to ENIG overplating, which was a result of palladium poisoning of ILD during M1 SAP. Improved fine line profile using a Ti-Cu SAP and high accuracy microvia ablation with fully filled via plating was confirmed by cross section after assembly.

Time zero electrical yield was measured using 17 test coupons across three panels after completing panel level 2.5-D assembly. The test sample size included:

- P1: 300 μm thick panel with eight assembled coupons (fully populated).
- P3: 300 μm thick panel with seven assembled coupons (partially populated).
- P5: 100 μm thick quarter-panel with two assembled coupons (partially populated).

Three test structure were analyzed including:

1. D2D: Fine-line die-to-die daisy chain (Figure 90).
2. M1-Die: Corner daisy chain (Figure 91 – upper left).
3. M1-M2-Die: Corner daisy chain and peripheral I/O daisy chain (Figure 91 – bottom left and right).

The pass condition for each test structure was a daisy chain resistance $R < 50\ \Omega$. An elevated pass condition was used based on coupon cross sections indicating solder depletion and line narrowing, which increased chip-level interconnection resistance. Figure 104 summarizes 2.5-D glass interposer yield after chip-level assembly according to the coupon map provided in Figure 105.

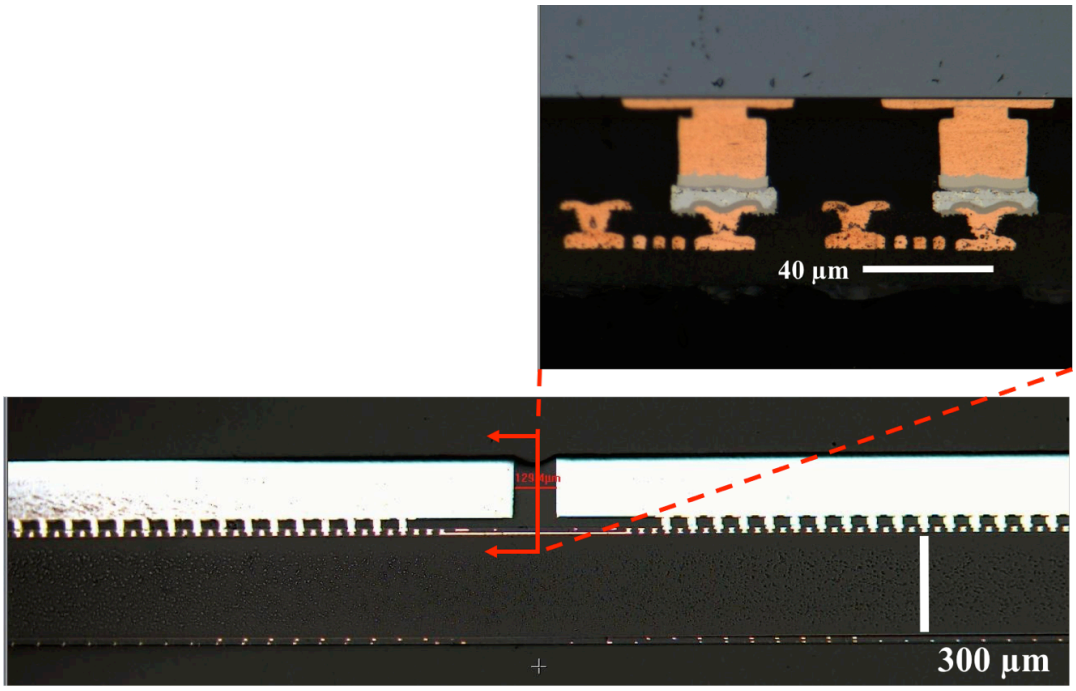


Figure 102. Chip level assembly on 300 µm glass without TPV.

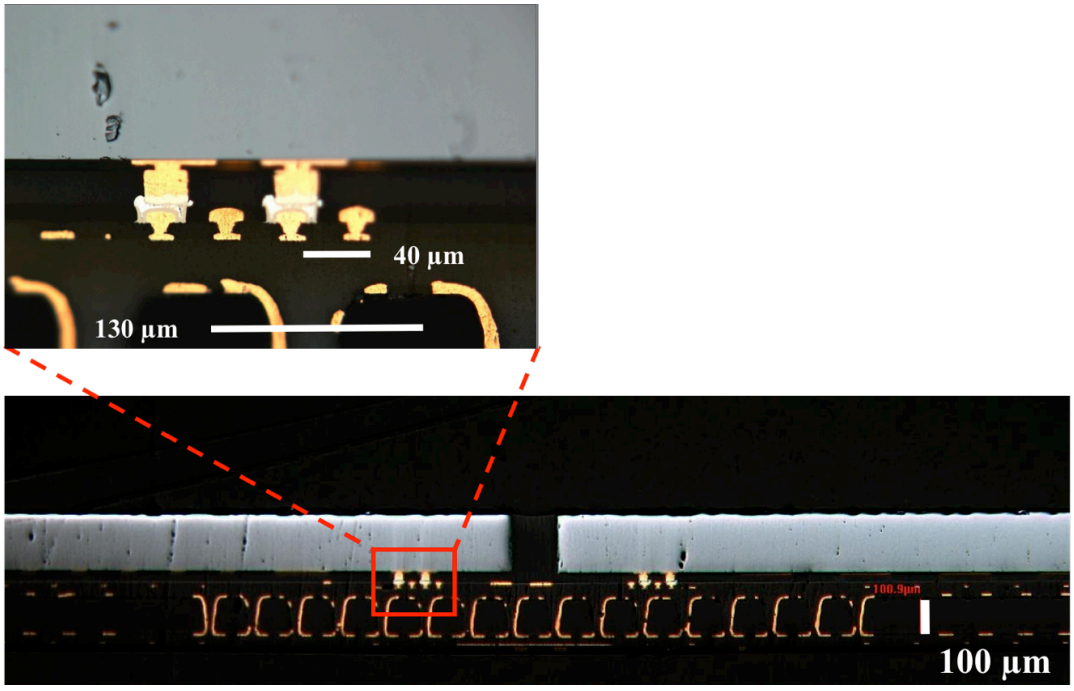


Figure 103. Chip level assembly on 100 µm glass with TPV.

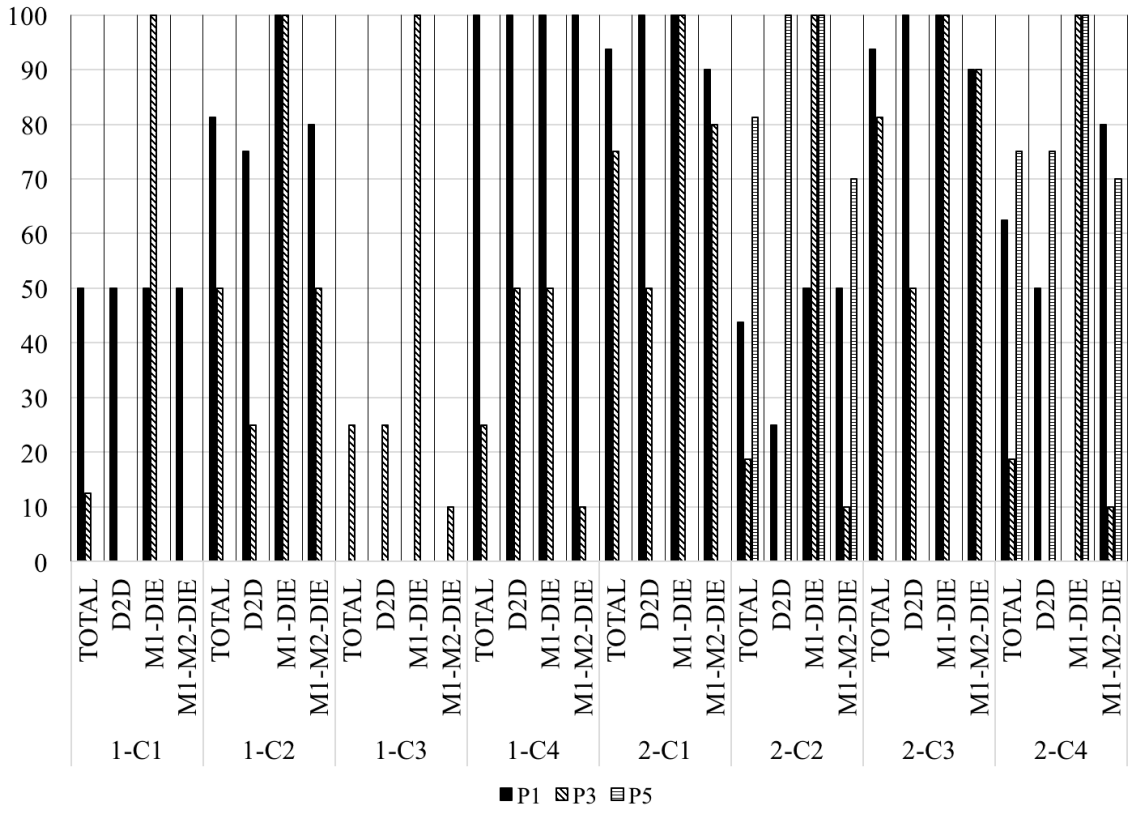


Figure 104. 2.5-D glass interposer yield after chip-level assembly on panel.

Coupon 1-C4 on P1 exhibited 1.00 yield for all test structures considered, indicating the first successful demonstration chip-level assembly on a 2.5-D glass interposer with fine pitch RDL. The average yield of test structure M1-Die for the 17 coupons tested was 0.875 indicating good 2.5-D TCB despite solder depletion. Test structure D2D yield is summarized in Figure 105 by average yield based on coupon position.

Panels considered for the reported time zero yield analysis used an e-less SAP flow. Therefore, over-etching of RDL traces during seed layer removal on M2 was considered the yield limiting process. The yield map in Figure 105 supports this

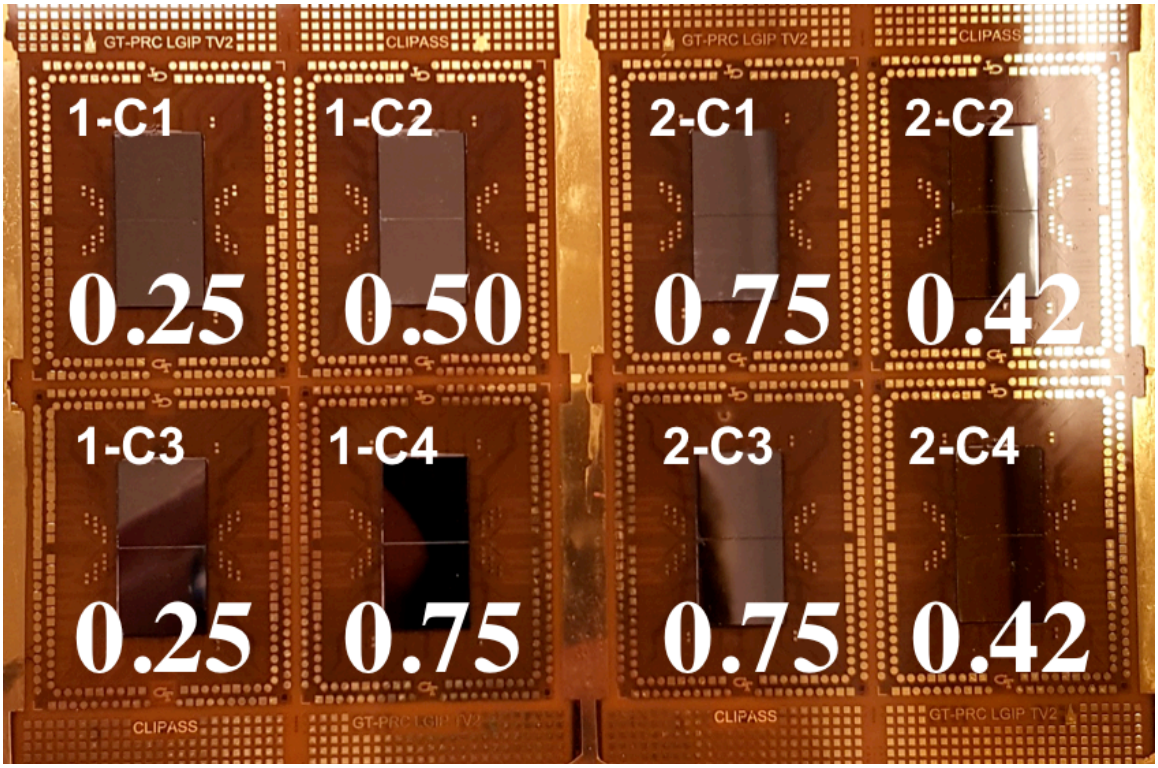


Figure 105. Coupon and die-to-die yield map.

conclusion since coupons near the panel edge exhibited lower D2D yield. Over-etching was a direct result of thinner copper after electrolytic plating due to decreased plating current density at the panel edge.

5.5 Summary

Modeling, design, fabrication, and characterization of wide and external I/O RDL test vehicles verified design rules to meet electrical performance targets summarized in Table 2. This chapter described the first fully integrated process demonstrator with RDL design rules required to address the electrical design challenges of a 2.5-D glass interposer package. Specifically, the integration of 6 µm pitch RDL lines, 8 µm microvias

at 40 μm pitch, and thermocompression bond was demonstrated using a double-sided SAP on 100 μm thick, 150 mm x 150 mm size glass panels with via-first, 60 μm TPVs at 130 μm pitch. Fully integrated fine-pitch RDL and 2.5-D chip-level assembly tests indicated up to 1.00 time-zero yield, and thus demonstrated, for the first time, a complete 2.5-D glass interposer process test vehicle.

Two fabrication technologies were shown to increase die-to-die interconnect density—(a) scaling microvia padstack to via-in-line dimensions consistent with the wide I/O design roadmap and (b) fully-filled microvias for via-in-pad die escape with multiple high density routing layers. Electrical test and optical inspection were used to confirm high microvia yield with less than 2 μm overlay drill accuracy across multiple panels. Further scaling of the microvia padstack, therefore, was recommended to increase wide I/O channel density. Furthermore, electrolytic plating of microvias demonstrated fully filled vias capable of via-in-pad assembly at 40 μm CLI pitch, and stacked vias when scaling the RDL technologies discussed to a multilayer high density routing RDL geometry.

CHAPTER 6. CONCLUSIONS

This thesis presented a fundamental model and design study to demonstrate low latency die-to-die and low loss die-to-board interconnects for the first time on a 2.5-D glass interposer package substrate. Based on these fundamental design studies, electrical design guidelines were established and integrated using RDL fabrication and chip-level assembly panel processes developed by other researchers into the first 2.5-D glass interposer package prototype. The 2.5-D glass interposer package demonstrated has the potential to address the performance, cost, and interconnect density requirements for future high performance computing systems.

Performance and cost benefits of transistor scaling leading to SoC slowed and was unable to meet system needs for heterogeneous die integration. Multi-die integration on package provided the optimum balance of performance and cost compared to chip- or board-level integration using standard I/O between FC-BGA packaged devices. Side-by-side multi-chip integration using 2.5-D interposers has become the preferred approach for such bandwidth scaling, due to the thermal and cost limitations of 3-D IC stacking. Although silicon interposers provide short ($L \approx 5$ mm), high density ($\delta \approx 500$ lines/mm) interconnects between multiple ICs, BEOL design rules and TSV losses limited electrical performance of die-to-die interconnects and die-to-board interconnects respectively. Furthermore, small 300 mm wafers and expensive fabrication processes increased the cost of silicon interposers.

The 2.5-D glass interposer package explored and demonstrated in this dissertation leverages the unique electrical, thermal, and mechanical properties of glass, as well as its

availability in thin and large panels, to achieve interconnect densities comparable to wafer-based silicon interposers at an estimated 2 – 5x lower cost using double-sided, panel-scalable processes.

The research objective of this thesis was to model, design, fabricate, and characterize high density, die-to-die (wide I/O) and high speed, die-to-board (external I/O) interconnections to achieve terabit per second bandwidth on 2.5-D glass interposer packages. Two major electrical design challenges were identified including: (a) low latency, wide I/O interconnections between ICs and (b) low loss, external I/O interconnections between the IC and board. Fundamental research tasks in electrical modeling and design were identified to address these challenges. The modeling and design of high density, low-latency RDL for wide I/Os and high speed, low-loss RDL for external I/Os was studied. In doing so, a design roadmap for the RDL structure of a 2.5-D glass interposer package was established. The design rules for each respective signal regime were then validated using glass RDL test vehicles, fabricated using panel processes.

In addition to these fundamental research tasks to address the wide I/O and external I/O electrical design challenges, an integration research task culminated in an initial process demonstration of a 2.5D glass interposer combining multilayer RDL with through vias in glass and fine pitch chip level interconnections. This chapter summarizes the research results, presents the significant scientific and technical contributions, and identifies future research directions in 2.5D glass interposer packages.

Table 9. Research tasks, targets, and results summary.

	Research Tasks	Targets	Results
Design	Wide I/O: high density, low latency RDL	< 0.02 UI/mm (2 Gbps)	0.013 UI/mm simulated 0.012 UI/mm measured
	External I/O: high speed, low loss RDL	< -0.1 dB/mm (14 GHz)	-0.03 dB/mm simulated -0.05 dB/mm measured
Demonstration	2.5-D glass interposer package chip-to-package (C2P) pitch	40 μm (C2P)	40 μm via-in-pad RDL 56 μm C2P TCB

6.1 Summary of Results

The electrical design and demonstration of a 2.5-D glass interposer research results are summarized in Table 9. All research targets outlined at the beginning of this dissertation research were achieved, addressing all the fundamental and integration challenges.

6.1.1 Low Latency Wide I/O

The RDL geometry and interposer stack-up for die-to-die interconnects was studied to reduce wide I/O latency. High aspect ratio interconnects were required to increase conductor cross section and reduce interconnect resistance per unit length by up to 4x compared to BEOL silicon interposers. The effect of conductor cross section on line capacitance and inductance was studied as a function of line width and height. Based on

this study, the design roadmap for wide I/O was established to reduce interconnect delay and effectively increase bandwidth per channel. Wide I/O latency was shown to decrease with increasing copper thickness to signal width aspect ratio. Furthermore, interconnect delay per unit length was shown to vary indirectly with $\sqrt[5]{A}$, where A was the conductor cross section, and A greater than 5 μm^2 was required to reduce latency below BEOL silicon interposer. Design rules for minimum line pitch and width were set according to microvia padstack dimensions to escape route chip-level I/Os at the targeted 40 μm pitch. Wide I/O bus simulation, which included crosstalk induced jitter, verified these design guidelines to achieve latencies as low as 0.013 UI/mm at 2 Gbps.

Design rules for low latency wide I/O were validated on a glass test vehicle fabricated using panel processes. The modeling and design of wide I/O showed that high copper thickness to line width aspect ratio to achieve greater than A = 5 μm^2 conductor cross section was required. The glass test vehicle leveraged a semi-additive process to increase copper thickness on glass and achieve up to A = 22 μm^2 at line width W = 2.2 μm. Meanwhile, the high elastic modulus and dimensional stability of glass allowed the scaling of RDL line pitch to achieve interconnect densities close to that of wafer-based silicon interposers. High frequency characterization of CPW (ground-signal-ground) test structures was used to verify isolated line delay as low as 0.012 UI/mm at 2 Gbps with a -3 dB bandwidth beyond 30 GHz. Therefore, data rates beyond 2 Gbps at line lengths greater than 10 mm are feasible using a glass interposer package to accommodate future high speed wide I/O die-to-die interconnections.

6.1.2 Low Loss External I/O

Differential traces directly on glass were studied to show the effect of line geometry on differential insertion loss and crosstalk. Low loss channels were developed using RDL directly on the surface of glass to improve conductor and dielectric losses. Surface roughness R_a less than 5 nm, loss tangent $tan\ \delta$ = 0.005 at 20 GHz, and larger conductor cross sections greater than 100 μm^2 improved line attenuation up to 10x compared to silicon. Modeling and simulation of edge coupled microstrip differential pairs showed that line attenuation as low as -0.03 dB/mm was achieved, and that minimum differential pair bend radius did not significantly increase insertion loss at die breakout. Matching the line pitch to chip level interconnect and through package via pitches was used to reduce differential impedance mismatch at these signal transitions. Lastly minimum pair spacing to achieve broadband crosstalk specifications was studied.

Differential pair line pitch, width, and pair spacing were validated using glass test vehicles fabricated using panel processes on bare, via-first glass. Skin effect and increased seed layer resistivity was shown to increase line attenuation by up to 70%. The fabricated RDL structures on glass showed line attenuation as low as -0.05 dB/mm at 14 GHz. High frequency characterization and eye diagram simulations at 28 Gbps NRZ were used to verify low loss at TPV transitions. The channel performance was compared with and without TPV transitions using measured S-parameters and high speed transceiver behavioral models. Time domain simulations showed 0.86 UI eye opening at BER = $1x10^{-12}$ without equalization. High frequency characterization verified differential pair spacing greater than 200 μm was required to achieve less than -30 dB differential crosstalk up to 40 GHz on 140 μm thick glass.

6.1.3 Design and Demonstration Test Vehicle

Modeling, design, fabrication, and characterization of wide and external I/O RDL test vehicles verified design rules to meet electrical performance targets summarized in Table 9. As a last step, the integration of 6 μm pitch RDL lines, 8 μm microvias at 40 μm pitch, and thermocompression bond was demonstrated on 100 μm thick, 150 mm x 150 mm size glass panels with via-first, 60 μm TPVs at 130 μm pitch. Fully integrated fine-pitch RDL and 2.5-D chip-level assembly tests indicated up to 1.00 time-zero yield, and thus demonstrated, for the first time, a complete 2.5-D glass interposer test vehicle.

This first fully integrated process demonstrator was used to demonstrate high density, wide I/O interconnects. Two fabrication technologies were shown to increase die-to-die interconnect density—(a) scaling microvia padstack to via-in-line dimensions consistent with the wide I/O design roadmap and (b) fully-filled microvias for via-in-pad die escape with multiple high density routing layers. Electrical test and optical inspection were used to confirm high microvia yield with less than 2 μm overlay errors across multiple panels. Further scaling of the microvia padstack, therefore, was recommended to increase wide I/O channel density. Furthermore, electrolytic plating of microvias demonstrated fully filled vias capable of via-in-pad assembly at 40 μm CLI pitch, and stacked vias when scaling the RDL technologies discussed to a multilayer high density RDL geometry.

6.2 Technical and Scientific Contributions

The major technical and scientific contributions from this thesis with the development of a 2.5-D glass interposer package as a superior alternative to silicon and organic interposers for HPC applications included:

1. Design and demonstration of low latency, wide I/O demonstrating line delay reduction up to 2x compared to BEOL silicon interposers using high aspect ratio channels routed in low loss build-up dielectrics.
2. Design and demonstration of low loss external I/Os demonstrating line attenuation reduction up to 10x compared to BEOL silicon interposer using RDL traces on glass with matched line, TPV, and CLI pitch.
3. First electrical design and integrated process demonstration of a 2.5-D glass interposer with:
    a. Yield-cognizant design rule developed and validated using RDL glass test vehicles.
    b. High interconnect density comparable to BEOL RDL at lower signal latency demonstrated using large panel processes comparable to HVM of organic package substrates.

The modeling, design, fabrication, and characterization of high density RDL for low latency wide I/O showed that high copper height to line width ratio was required to reduce latency, and line pitch and width comparable to silicon BEOL was achieved on glass panels.

The modeling, design, fabrication, and characterization of high speed RDL for low loss external I/O showed that matching differential line pitch to TPV and CLI bump pitch

improved signal integrity and fine pitch TPV in thin via-first glass panel are electrically transparent at 14 GHz.

These RDL technologies were integrated and demonstrated for the first time on a glass interposer fabricated using double-sided, panel-scalable processes with fine pitch chip-level assembly on panel. In doing so, a 2.5-D glass interposer capable of meeting next generation HPC system requirements was demonstrated. Using the 2.5-D glass interposer package approach, terabit per second bandwidth between die is feasible using low latency wide I/O RDL scalable to data rates above 2 Gbps/channel. Furthermore, high bandwidth density for external I/O is possible using low loss external I/O with low loss TPV at data rate above 28 Gbps/channel.

6.3 Recommendations for Future Work

This research made key initial contributions towards the development of a 2.5-D glass interposer package to address the performance and cost challenges of wafer-based silicon interposers and the interconnect scaling challenges of organic interposers. A set of electrical design guidelines for signal integrity of a 2.5-D glass interposer package was developed as a part of this thesis. Although this thesis developed initial solutions to two major electrical design challenges and demonstrated a preliminary 2.5-D glass interposer test vehicle with coarser design rules, significant future research needs to be done in substrate and assembly processes to realize the aggressive design rules required to meet the 2.5D interposer roadmap. Three specific areas were identified for further improvement and future work discussed in this section below.

The design of low latency die-to-die interconnects showed that scaling microvia padstack was critical to increase wide I/O interconnection density. Scaling microvia padstack to achieve via-in-line capability is required. Extensive electrical characterization of new dielectric materials and RDL processes is required. Maintaining low latency wide I/O interconnects requires high aspect ratio lines in low permittivity build-up dielectrics to effectively reduce line resistance and capacitance. Furthermore, the demonstration of low latency RDL was shown for a single fine line SAP layer. Scaling this technology to at least two signal routing layers using a signal-ground-signal stack-up for wide I/O can significantly increase die-to-die bandwidth.

The line attenuation for external I/O was significantly improved using RDL on glass. Line performance and bandwidth density can be further improved by reducing glass interposer thickness. Differential pair spacing to maintain crosstalk budgets will decrease, and the effect of TPV on signal integrity will be minimal, which is required to further scale data rates up to and beyond 56 Gbps. In addition to improving RDL on glass performance, characterizing the full path including CLI breakout to the glass routing layer is required, and will require optimization of microvia and pin assignment to maintain signal integrity.

Further characterization of larger-than-reticle glass interposer packages directly attached to the PWB is required. Recently, the mechanical reliability of the 2.5-D glass interposer package has been studied and high CTE glass was shown to improve chip- and board- level reliability. Continued efforts are required to quantify the reliability not only for interconnection reliability, but also fine line reliability. Furthermore, the signal and

power integrity advantages of a 2.5-D glass interposer package mounted directly to the PWB can be explored.

6.4 Lists of Publications

6.4.1 Journal Publications

B. Sawyer, Y. Suzuki, R. Furuya, C. Nair, T. Huang, V. Smet, K. Panayappan, V. Sundaram, R. Tummala, "Design and Demonstration of a 2.5D Glass Interposer BGA Package for High Bandwidth and Low Cost," IEEE TCPMT, 2017.

B. Sawyer, Y. Suzuki, Z. Wu, H. Lu, V. Sundaram, K. Panayappan, R. Tummala, "Design and Demonstration of Fine-Pitch and High- Speed Redistribution Layers for Panel-Based Glass Interposers at 40-micron Bump Pitch," JMEP, 2016.

H. Lu, R. Furuya, ***B. Sawyer***, C. Nair, F. Liu, V. Sundaram, R. Tummala, "Design, Modeling, Fabrication and Characterization of 2 - 5 Micron Redistribution Layer Traces by Advanced Semi-Additive Processes on Low Cost Panel-Based Glass Interposers," IEEE TCPMT, 2016.

6.4.2 Conference Publications

B. Sawyer, B. Chou, J. Tong, W. Vis, K. Panayappan, V. Sundaram, R. Tummala, "Design and Demonstration of 28 Gbps Signal Transmission on Glass Panel as a Lower Cost and Higher Performance Alternative to Silicon," IEEE ECTC, 2016.

B. Sawyer, B. Chou, S. Ghandi, J. Mateosky, V. Sundaram, R. Tummala, “Modeling, Design, and Demonstration of 2.5D Glass Interposers for 16-channel 28 Gbps Signaling Applications,” IEEE ECTC, 2015.

B. Sawyer, H. Lu, Y. Suzuki, Y. Takagi, M. Kobayashi, V. Smet, T. Sakai, V. Sundaram, R. Tummala, “Modeling, Design, Fabrication and Characterization of First Large 2.5D Glass Interposer as a Superior Alternative to Silicon and Organic Interposers at 50-micron bump pitch," IEEE ECTC, 2014.

H. Lu, R. Furuya, ***B. Sawyer,*** C. Nair, F. Liu, V. Sundaram, R. Tummala, “Design, Modeling, Fabrication and Characterization of 2 - 5 Micron Redistribution Layer Traces by Advanced Semi-Additive Processes on Low Cost Panel-Based Glass Interposers,” IEEE TCPMT, 2016.

T. Sakai, ***B. Sawyer***, H. Lu, Y. Takagi, R. Furuya, Y. Suzuki, M. Kobayashi, V. Smet, V. Sundaram, R. Tummala, “Design and Demonstration of Large 2.5D Glass Interposer for High Bandwidth Applications,” ICSJ, 2014.

REFERENCES

[1] S. Jiva, "Datacenter Networking Memory Solutions: Where Mainstream and High Performance Intersect," in *MEMCON*, Santa Clara, CA, 2016.

[2] B. Bottoms, "Maintaining The Pace of Progress As We Approach The End Of Moore's Law: New Materials, New Processes, New Architectures," presented at the International Symposium on Microelectronics, Orlando, FL, 2015.

[3] M. Deo, "Enabling Next-Generation Platforms Using Altera's 3D System-in-Package Technology," Altera,WP-01251, 2015.

[4] L. Li *et al.*, "Addressing bandwidth challenges in next generation high performance network systems with 3D IC integration," in *2012 IEEE 62nd Electronic Components and Technology Conference*, 2012, pp. 1040-1046.

[5] K. Saban, "Xilinx Stacked Silicon Interconnect Technology Delivers Breakthrough FPGA Capacity, Bandwidth, and Power Efficiency," Xilinx, White Paper: Virtex-7 FPGA WP380, 2012.

[6] N. Kim, D. Wu, D. Kim, A. Rahman, and P. Wu, "Interposer design optimization for high frequency signal transmission in passive and active interposer using through silicon via (TSV)," in *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*, 2011, pp. 1160-1167.

[7] R. R. Tummala, *Introduction to system-on-package (SOP) miniaturization of the entire system*. New York: McGraw-Hill, 2008.

[8] J. U. Knickerbocker *et al.*, "3D silicon integration," in *2008 58th Electronic Components and Technology Conference*, 2008, pp. 538-543.

[9] J. U. Knickerbocker *et al.*, "2.5D and 3D technology challenges and test vehicle demonstrations," in *2012 IEEE 62nd Electronic Components and Technology Conference*, 2012, pp. 1068-1076.

[10] J. U. Knickerbocker *et al.*, "3-D Silicon Integration and Silicon Packaging Technology Using Silicon Through-Vias," *IEEE Journal of Solid-State Circuits,* vol. 41, no. 8, pp. 1718-1725, 2006.

[11] H. Lee *et al.*, "Design and signal integrity analysis of high bandwidth memory (HBM) interposer in 2.5D terabyte/s bandwidth graphics module," in *2015 IEEE*

24th Electrical Performance of Electronic Packaging and Systems (EPEPS), 2015, pp. 145-148.

[12] C. C. Lee *et al.*, "An Overview of the Development of a GPU with Integrated HBM on Silicon Interposer," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 1439-1444.

[13] *High Bandwidth Memory (HBM) DRAM*, JESD235, 2013.

[14] N. Kim, D. Wu, J. Carrel, J. H. Kim, and P. Wu, "Channel design methodology for 28Gb/s SerDes FPGA applications with stacked silicon interconnect technology," in *2012 IEEE 62nd Electronic Components and Technology Conference*, 2012, pp. 1786-1793.

[15] D. C. Hu, Y. P. Hung, Y. H. Chen, R. M. Tain, and W. C. Lo, "Embedded glass interposer for heterogeneous multi-chip integration," in *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, 2015, pp. 314-317.

[16] Y. Deng and W. Maly, "2.5D system integration: a design driven system implementation schema," in *ASP-DAC 2004: Asia and South Pacific Design Automation Conference 2004 (IEEE Cat. No.04EX753)*, 2004, pp. 450-455.

[17] Y. Deng and W. Maly, "A feasibility study of 2.5D system integration," in *Proceedings of the IEEE 2003 Custom Integrated Circuits Conference, 2003.*, 2003, pp. 667-670.

[18] J. Priest, M. Ahmad, L. Li, X. Jie, and M. Brillhart, "Design optimization of a high performance FCAMP package for manufacturability and reliability," in *Proceedings Electronic Components and Technology, 2005. ECTC '05.*, 2005, pp. 1497-1499 Vol. 2.

[19] C. L. Pan, Y. J. Huang, and C. Y. Wang, "Characterization and simulation for 2.5-D interposer," in *2015 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)*, 2015, pp. 74-77.

[20] S. W. Ho *et al.*, "2.5D through silicon interposer package fabrication by chip-on-wafer (CoW) approach," in *2014 IEEE 16th Electronics Packaging Technology Conference (EPTC)*, 2014, pp. 679-683.

[21] L. Li, M. Higashi, A. Takano, J. Xue, and G. Ikari, "Cost and performance effective silicon interposer and Vertical Interconnect for 3D ASIC and memory integration," in *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, 2014, pp. 1366-1371.

[22] M. Ishida, "APX (Advanced Package X) - Advanced Organic Technology for 2.5D Interposer," in *Electronic Components and Technology Conference*, Orlando, FL, 2014.

[23] L. Li *et al.*, "3D SiP with Organic Interposer for ASIC and Memory Integration," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 1445-1450.

[24] K. Oi *et al.*, "Development of new 2.5D package with novel integrated organic interposer substrate with ultra-fine wiring and high density bumps," in *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, 2014, pp. 348-353.

[25] R. Mahajan *et al.*, "Embedded Multi-die Interconnect Bridge (EMIB) -- A High Density, High Bandwidth Packaging Interconnect," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 557-565.

[26] C. K. Lee *et al.*, "Investigation of the process for glass interposer," in *2013 8th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, 2013, pp. 194-197.

[27] H. Lu *et al.*, "Design, Modeling, Fabrication and Characterization of 2–5 μm Redistribution Layer Traces by Advanced Semiadditive Processes on Low-Cost Panel-Based Glass Interposers," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. 6, no. 6, pp. 959-967, 2016.

[28] V. Sukumaran, T. Bandyopadhyay, V. Sundaram, and R. Tummala, "Low-Cost Thin Glass Interposers as a Superior Alternative to Silicon and Organic Interposers for Packaging of 3-D ICs," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. 2, no. 9, pp. 1426-1433, 2012.

[29] B. Singh *et al.*, "Demonstration of Enhanced System-Level Reliability of Ultra-Thin BGA Packages with Circumferential Polymer Collars and Doped Solder Alloys," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 1377-1385.

[30] J. U. Knickerbocker *et al.*, "System-on-package (SOP) technology, characterization and applications," in *56th Electronic Components and Technology Conference 2006*, 2006, p. 7 pp.

[31] A. Martwick, Drew, J. , "3D Stacked Signaling, Jitter and Measurement," presented at the DesignCon 2014, Santa Clara, CA, 29-30 January 2014, 2014.

[32] A. Martwick and J. Drew, "Silicon interposer and TSV signaling," in *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, 2015, pp. 266-275.

[33] A. Martwick, "HBM/WIO2 Electrical Signaling," 2012.

[34] R. Oikawa *et al.*, "A high-speed, long-reach signal design challenge for 2.5-D LSI based on a low-cost silicon interposer and a large-scale SSO analysis," in *2015*

IEEE 65th Electronic Components and Technology Conference (ECTC), 2015, pp. 293-300.

[35] K. Cho *et al.*, "Design and Analysis of Power Distribution Network (PDN) for High Bandwidth Memory (HBM) Interposer in 2.5D Terabyte/s Bandwidth Graphics Module," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 407-412.

[36] A. Wong, G. Tsui, B. K. Soo, C. L. Khoo, and Y. Wang, "High bandwidth low power interposer interconnect challenge, design, and validation in 3D silicon stacked interconnect (SSI) technology," in *2016 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2016, pp. 434-439.

[37] S. Choi *et al.*, "Eye-diagram estimation and analysis of High-Bandwidth Memory (HBM) interposer channel with crosstalk reduction schemes on 2.5D and 3D IC," in *2016 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2016, pp. 425-429.

[38] K. Cho *et al.*, "Design optimization of high bandwidth memory (HBM) interposer considering signal integrity," in *2015 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)*, 2015, pp. 15-18.

[39] H. Lee, K. Cho, H. Kim, S. Choi, J. Lim, and J. Kim, "Electrical performance of high bandwidth memory (HBM) interposer channel in terabyte/s bandwidth graphics module," in *2015 International 3D Systems Integration Conference (3DIC)*, 2015, pp. TS2.2.1-TS2.2.4.

[40] X. Gu *et al.*, "High-density silicon carrier transmission line design for chip-to-chip interconnects," in *2011 IEEE 20th Conference on Electrical Performance of Electronic Packaging and Systems*, 2011, pp. 27-30.

[41] Y. Jeon, H. Kim, S. Choi, Y. Kim, and J. Kim, "Design of an On-Interposer Passive Equalizer for High Bandwidth Memory (HBM) with 30Gbps Data Transmission," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 2475-2480.

[42] R. Oikawa, "A Feasibility Study on 100Gbps-Per-Channel Die-to-Die Signal Transmission on Silicon Interposer-Based 2.5-D LSI with a Passive Digital Equalizer," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 957-965.

[43] C. S. Patel *et al.*, "Silicon Carrier with Deep Through-Vias, Fine Pitch Wiring and Through Cavity for Parallel Optical Transceiver," in *Proceedings Electronic Components and Technology, 2005. ECTC '05.*, 2005, pp. 1318-1324.

[44] N. Kim, C. Shin, D. Wu, J. h. Kim, and P. Wu, "Performance analysis and optimization for silicon interposer with Through Silicon Via (TSV)," in *2012 IEEE International SOI Conference (SOI)*, 2012, pp. 1-2.

[45] E. Wu, K. Abugharbieh, B. Banijamali, S. Ramalingam, P. Wu, and C. Wyland, "Interconnect and package design of a heterogeneous stacked-silicon FPGA," in *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference*, 2013, pp. 1-8.

[46] Y. Kim, J. Cho, K. Kim, V. Sundaram, R. Tummala, and J. Kim, "Signal and power integrity analysis in 2.5D integrated circuits (ICs) with glass, silicon and organic interposer," in *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, 2015, pp. 738-743.

[47] H. B. Bakoglu, *Circuits, interconnections, and packaging for VLSI*. Reading, Massachusetts: Addison-Wesley, 1990.

[48] H. Lu *et al.*, "Demonstration of 3 - 5 um RDL line lithography on panel-based glass interposers," in *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, 2014, pp. 1416-1420.

[49] F. Michalik *et al.*, "EcoFlash: Next level of enhanced isotropic etchants," in *2015 10th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, 2015, pp. 83-87.

[50] E. Bogatin, *Signal and Power Integrity - Simplified*. New Jersey: Pearson Education 2010.

[51] A. Rahimi and Y. K. Yoon, "Integrated low loss RF passive components on glass interposer technology," presented at the 2015 IEEE 65th Electronic Components and Technology Conference (ECTC), 26-29 May 2015, 2015.

[52] V. Sukumaran *et al.*, "Design, Fabrication, and Characterization of Ultrathin 3-D Glass Interposers With Through-Package-Vias at Same Pitch as TSVs in Silicon," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. 4, no. 5, pp. 786-795, 2014.

[53] S. Takahashi, K. Horiuchi, K. Tatsukoshi, M. Ono, N. Imajo, and T. Mobely, "Development of Through Glass Via (TGV) formation technology using electrical discharging for 2.5/3D integrated packaging," in *2013 IEEE 63rd Electronic Components and Technology Conference*, 2013, pp. 348-352.

[54] T. Shi *et al.*, "Design, Demonstration and Characterization of Ultra-Thin Low-Warpage Glass BGA Packages for Smart Mobile Application Processor," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 1465-1470.